Commercial DT / M4.1 Chassis System
Project name: vHulk
SCH Ver: -1
PCB Number: 14065-1

PCB BOARD SIZE
4 Layer / 244 mm x 244 mm

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02	BLOCK DIAGRAM
03	CPU (PCIE/DMI)
04	CPU (CFG/CLOCK/PM)
05	CPU (DDR_CHA)
06	CPU (DDR_CHB)
07	CPU (DDI/EDP)
08	CPU (CPU Power)
09	CPU (VSS)
10	CPU (Power CAP)
11	DDR DIMM_2
12	DDR DIMM_1
13	DDR DIMM_4
14	DDR DIMM_3
15	PCH (SPI/UART/I2C)
16	PCH (DMI/PCI-E/USB)DDI GP
17	PCH (PCI-E/SATA)
18	PCH (CLOCK/CL)
19	PCH (USB/ESPI)
20	PCH(GPIO/CPU/SMBUS/IHDA/JTAG)
21	PCH (POWER1)
22	PCH (POWER2)_PCH Strap
23	PCH Power CAP
24	SIO_ITE8733
25	Flash&RTC
26	Thermal&FAN
27	Audio Codec_ALC662
28	AMP_(R)
29	Audio IO_Front
30	Audio IO_Rear
31	LAN_RTL8111EPV
32	RJ45&Transformer
33	Card Reader_(R)
34	USB Charger_(R)
35	USB_Redrive_(R)
36	USB20_REAR PORT
37	USB20_FRONT HEADER
38	USB30_REAR PORT
39	USB30_FRONT HEADER
40	Power Plane EN Sequence
41	Dual Power
42	Switch power
43	ATX(BATT Conn)
44	Power Sequence(DDR4)
45	DCDC-3D3V&5V
46	VCORE & V_GT IC(NCP81203)
47	VCORE OUTPUT (NCP81151)
48	V_GT OUTPUT(NCP81151)
49	5V &3.3V(RT8243A)
50	DDR_PWR (RT8207M)
51	PCH_1P0V(RT8237C)
52	VCC_SA(NCP5230M)
53	VCC_IO(RT8237C)
54	LDO_1P5V_1P8V_2P5V

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55	DVI-D
56	DP2
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59	PCI bridge
60	HDD/ODD
61	Mini card-WLAN
62	Mini card-SSD_(R)
63	Mini card-NGFF
64	Front board
65	Others
66	IO Board_(R)
67	COM
68	Debug
69	LPT
70	G sensor_(R)
71	Thunderbolt_(R)
72	Thunderbolt_(R)
73	Thunderbolt_(R)
74	Thunderbolt_(R)
75	Thunderbolt_(R)
76	GPU_(R)
77	GPU_(R)
78	GPU_(R)
79	GPU_(R)
80	GPU_(R)
81	GPU VRAM 1&2_(R)
82	GPU VRAM 3&4_(R)
83	GPU VRAM 5&6_(R)
84	GPU VRAM 7&8_(R)
85	GPU CORE_(R)
86	GPU discrete power_(R)
87	GPU Switch_(R)
88	GPU Switch_(R)
89	GPU others_(R)
90	NFC_(R)
91	TPM
92	PS2
93	Express Card
94	Smart Card
95	Scalar_(R)
96	MCU_(R)
97	Inter LAN
98	LAN Switch_(R)
99	XDP&ITP
100	Table of Content
101	GPIO table
102	POWER SEQUENCE
103	Power Block Diagram
104	SMBUS table
105	CLOCK MAP
106	RESET Flow CHART
107	Change History

Jomper SETTING

CMOS1	1-2 Short	With Jumper to Clear CMOS
WP1	1-2 Short	With Jumper to enable WP
OBR1	1-2 Open	Without Jumper to recovery
MECLR1	1-2 Short	With Jumper to enable ME

BOM Configuration

(R_) : unmount
(E_) : SATA Express
(Q_) : Q170
(B_) : B150
(D_) : VGA
(W_) : For WST/FXC MB
(T_) : TPM on board
(S_) : For ECS MB
(H_) : TPM header

Key IC

CPU1	Intel CPU Skylake S 65W
PCH1	Intel PCH Q170/B150
U7901	ITE SIO IT8733F-DX
U2701	RealTek Audio Codec ALC662-VD
U3	Realtek LAN RTL8111EPV-CG
TPM1	NuvoTon TPM NPCT650AAAWX
U72	INTEL LAN I219LM I219
U54	ITE PCI Bridge IC IT8893E
U6506	Realtek converter RTD2168-CG

Header

SPK1	21.63415.204
AUDF1	21.62895.205
FANC1	21.60626.104
FANS1	21.60626.104
CMOS1	21.61445.103
OBR1	21.60909.102
WP1	21.61445.103
PCHDR1	021.60235.0204
LPT1	021.60217.0213
COM1	21.62884.205
TPMH1	21.62900.210
CSOPN1	21.62874.102
MECLR1	21.61445.103

Power sates

	Name	G3	EUP	S5	S4	S3	S0
+12V	12V_S0						O
	12V_CPU_S0						
-12V	-12V_S0						O
5V	ATX_5VSB		O	O	O	O	O
	+5V_AUX1						
	+5V_AUX2			O	O	O	O
	5V_USB20_RJUSB2						
	5V_USB30P1						
	5V_USB30P2						
	5V_USB30H1						
	5V_USB20P1						
	5V_USB20_RJUSB1				O	O	O
	5V_USB20H2						
	5V_USB20H1						
	5V_USB30H2						
	5V_S0						O
	5V_DVI						
3.3V	ATX_3.3VSB		O	O	O	O	O
	3P3V_LAN						
	3P3V_S5						
	3D3V_VCCPGPPA_Sx						
	3D3V_1D8V_PCHSPI_Sx			O	O	O	O
	3D3V_DVDDIO_AUDIO						
	DVDD_IO						
	3D3V_S0						O
	3D3V_RTD2168						
3.0V	3V_VBAT1_G3						
	3V_VRTC_G3	O	O	O	O	O	O
	3D3V_VCCPRTC						
2.5V	2D5V_VPP				O	O	O
1.2V	VDDQ				O	O	O
DIMM	DDR_VTT					O	O
PCH	1D0V_S5						
	1V_VCCF24_Sx						
	1V_VCCAMPHYPLL_Sx			O	O	O	O
	1V_VCCAPLL_Sx						
CPU	VCC_CORE						
	GFX_CORE						
	VCC_SA						O
	VCC_IO						
	1V_VCCST_VCCPLL_S3					O	O

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Title: COVER PAGE

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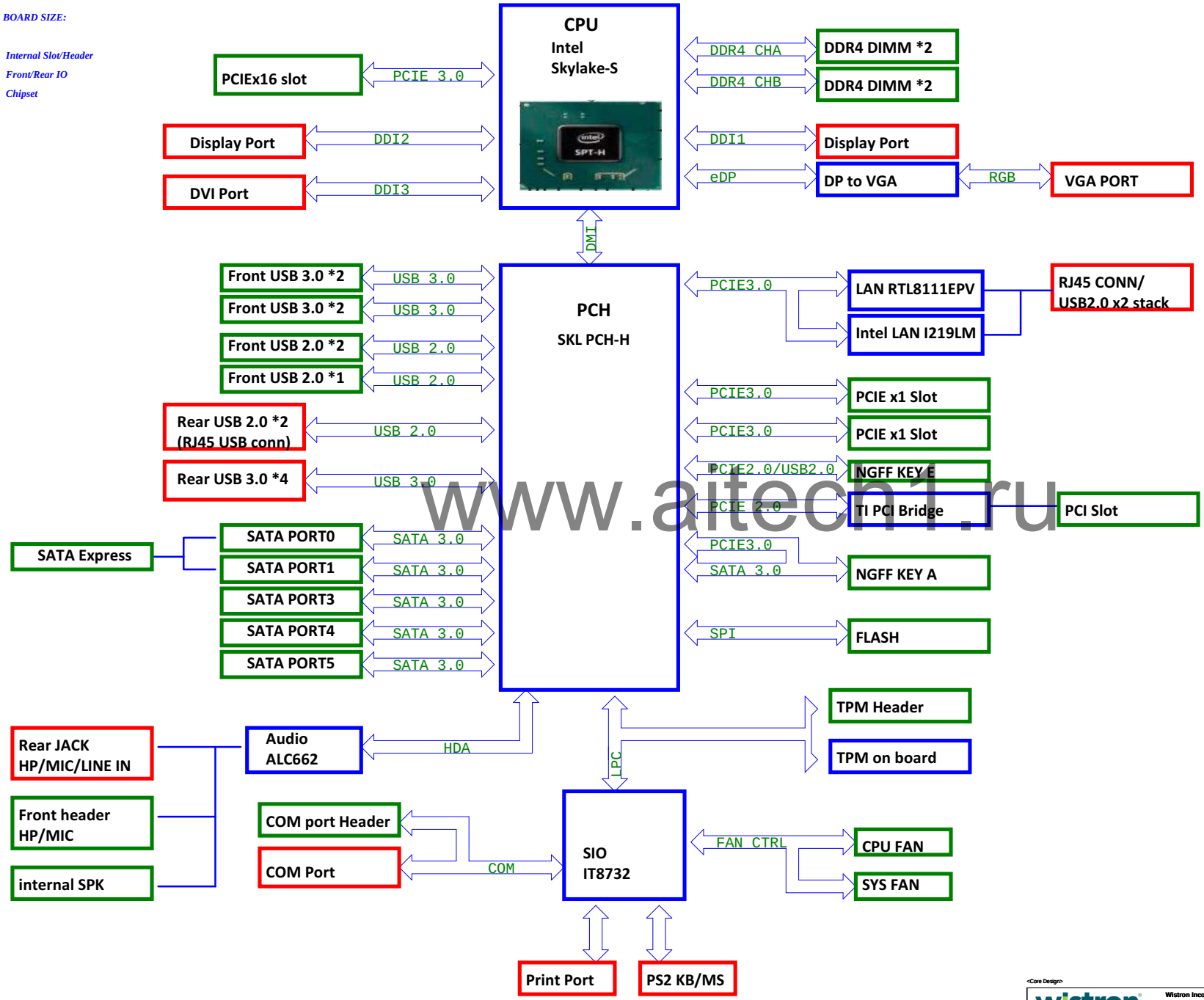
Date: Wednesday, September 23, 2015 | Sheet 1 of 107

PROJECT NAME: vHULK
MB VERSION: -1

PCB BOARD SIZE:

- *Internal Slot/Header*
- *Front/Rear IO*
- *Chipset*



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Hsichih, Taipei Hsien

Title: BLOCK DIAGRAM

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PEG

93 PEG_TX_CPU_P[0..15]
93 PEG_TX_CPU_N[0..15]
93 PEG_RX_CPU_P[0..15]
93 PEG_RX_CPU_N[0..15]

DMI

16 DMI_RX_CPU_P[0..3]
16 DMI_RX_CPU_N[0..3]
16 DMI_TX_CPU_P[0..3]
16 DMI_TX_CPU_N[0..3]

CPU1C 3 OF 12

SKYLAKE

LGA1151

PEG_RX_CPU_P0	B8	PEG_RXP0	PEG_TXP0	A5	PEG_TX_CPU_P0
PEG_RX_CPU_N0	B7	PEG_RXN0	PEG_TXN0	A6	PEG_TX_CPU_N0
PEG_RX_CPU_P1	C7	PEG_RXP1	PEG_TXP1	B4	PEG_TX_CPU_P1
PEG_RX_CPU_N1	C6	PEG_RXN1	PEG_TXN1	B5	PEG_TX_CPU_N1
PEG_RX_CPU_P2	D6	PEG_RXP2	PEG_TXP2	C3	PEG_TX_CPU_P2
PEG_RX_CPU_N2	D5	PEG_RXN2	PEG_TXN2	C4	PEG_TX_CPU_N2
PEG_RX_CPU_P3	E5	PEG_RXP3	PEG_TXP3	D2	PEG_TX_CPU_P3
PEG_RX_CPU_N3	E4	PEG_RXN3	PEG_TXN3	D3	PEG_TX_CPU_N3
PEG_RX_CPU_P4	F6	PEG_RXP4	PEG_TXP4	E1	PEG_TX_CPU_P4
PEG_RX_CPU_N4	F5	PEG_RXN4	PEG_TXN4	E2	PEG_TX_CPU_N4
PEG_RX_CPU_P5	G5	PEG_RXP5	PEG_TXP5	F2	PEG_TX_CPU_P5
PEG_RX_CPU_N5	G4	PEG_RXN5	PEG_TXN5	F3	PEG_TX_CPU_N5
PEG_RX_CPU_P6	H6	PEG_RXP6	PEG_TXP6	G1	PEG_TX_CPU_P6
PEG_RX_CPU_N6	H5	PEG_RXN6	PEG_TXN6	G2	PEG_TX_CPU_N6
PEG_RX_CPU_P7	J5	PEG_RXP7	PEG_TXP7	H2	PEG_TX_CPU_P7
PEG_RX_CPU_N7	J4	PEG_RXN7	PEG_TXN7	H3	PEG_TX_CPU_N7
PEG_RX_CPU_P8	K6	PEG_RXP8	PEG_TXP8	J1	PEG_TX_CPU_P8
PEG_RX_CPU_N8	K5	PEG_RXN8	PEG_TXN8	J2	PEG_TX_CPU_N8
PEG_RX_CPU_P9	L5	PEG_RXP9	PEG_TXP9	K2	PEG_TX_CPU_P9
PEG_RX_CPU_N9	L4	PEG_RXN9	PEG_TXN9	K3	PEG_TX_CPU_N9
PEG_RX_CPU_P10	M6	PEG_RXP10	PEG_TXP10	L1	PEG_TX_CPU_P10
PEG_RX_CPU_N10	M5	PEG_RXN10	PEG_TXN10	L2	PEG_TX_CPU_N10
PEG_RX_CPU_P11	N5	PEG_RXP11	PEG_TXP11	M2	PEG_TX_CPU_P11
PEG_RX_CPU_N11	N4	PEG_RXN11	PEG_TXN11	M3	PEG_TX_CPU_N11
PEG_RX_CPU_P12	P6	PEG_RXP12	PEG_TXP12	N1	PEG_TX_CPU_P12
PEG_RX_CPU_N12	P5	PEG_RXN12	PEG_TXN12	N2	PEG_TX_CPU_N12
PEG_RX_CPU_P13	R5	PEG_RXP13	PEG_TXP13	P2	PEG_TX_CPU_P13
PEG_RX_CPU_N13	R4	PEG_RXN13	PEG_TXN13	P3	PEG_TX_CPU_N13
PEG_RX_CPU_P14	T6	PEG_RXP14	PEG_TXP14	R2	PEG_TX_CPU_P14
PEG_RX_CPU_N14	T5	PEG_RXN14	PEG_TXN14	R1	PEG_TX_CPU_N14
PEG_RX_CPU_P15	U5	PEG_RXP15	PEG_TXP15	T2	PEG_TX_CPU_P15
PEG_RX_CPU_N15	U4	PEG_RXN15	PEG_TXN15	T3	PEG_TX_CPU_N15

VCC_IO

R302 1 2 24D9R2F-L-GP

PEG_RCOMP_CPU L7

PEG_RCOMP

DMI_RX_CPU_P0	Y3	DMI_RXP0	DMI_TXP0	AC2	DMI_TX_CPU_P0
DMI_RX_CPU_N0	Y4	DMI_RXN0	DMI_TXN0	AC1	DMI_TX_CPU_N0
DMI_RX_CPU_P1	AA4	DMI_RXP1	DMI_TXP1	AD3	DMI_TX_CPU_P1
DMI_RX_CPU_N1	AA5	DMI_RXN1	DMI_TXN1	AD2	DMI_TX_CPU_N1
DMI_RX_CPU_P2	AB4	DMI_RXP2	DMI_TXP2	AE2	DMI_TX_CPU_P2
DMI_RX_CPU_N2	AB3	DMI_RXN2	DMI_TXN2	AE1	DMI_TX_CPU_N2
DMI_RX_CPU_P3	AC4	DMI_RXP3	DMI_TXP3	AF2	DMI_TX_CPU_P3
DMI_RX_CPU_N3	AC5	DMI_RXN3	DMI_TXN3	AF3	DMI_TX_CPU_N3

SKYLAKE-1

FOXCONN: 062.10015.0081
LOTES: 062.10015.0111

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CPU XDP

XDP_PCUDEBUG<3>

CFG[0..15]
SKL_PCUSTB_0_DP
SKL_PCUSTB_0_DN
SKL_PCUSTB_1_DP
SKL_PCUSTB_1_DN

BPM_CPU_N0
BPM_CPU_N1

H_TDO
H_TDI
H_TMS
H_TCK

H_TRST_N
H_PREQ_N
H_PRDY_N

SVID

46 VIDSCK_VR1
46 VIDSOUT_VR1
46 VIDALERT#_VR1

CLOCK

18 CPU_BCLK_PCH
18 CPU_BCLK_PCH#

18 CPU_PCIBCLK_PCH
18 CPU_PCIBCLK_PCH#

18 CPU_CLK24M_PCH
18 CPU_CLK24M_PCH#

CONTROL

46 PROCHOT#_R
44 DDR_VTT_CNTL
40 CPU_VCCST_PWRGD
20 H_PWRGD
17 PLTRST_CPU_N
17 PM_SYNC_CPU
17 PM_DOWN_PCH
17,24 PECI_CPU
17 THERMTRIP#_CPU_R
16 H_SKTOCC_N

CFG3 — R414 1KR2J-1-GP — XDP_PCUDEBUG<3>

CPU1E — SKYLAKE — 5 OF 12 — LGA1151 — SKYLAKE-1

CPU_BCLK_PCH W5 → BCLKP
CPU_BCLK_PCH# W4 → BCLKN
CPU_PCIBCLK_PCH W1 → PCI_BCLKP
CPU_PCIBCLK_PCH# W2 → PCI_BCLKN
CPU_CLK24M_PCH K9 → CLK24P
CPU_CLK24M_PCH# J9 → CLK24N

VIDALERT#_VR1 — R469 220R2J-L2-GP — VIDALERT#_CPU E39 → VIDALERT#
VIDSCK_VR1 E38 → VIDSCK
VIDSOUT_VR1 E40 → VIDSOUT
PROCHOT#_R — R467 100R2J-2-GP — PROCHOT#_CPU C39 → PROCHOT#

DDR_VTT_CNTL AC36 → DDR_VTT_CNTL
TP_CPU_ZVM# AC38 → ZVM#
TP_CPU_AC37 AC37 → RSVD_AC37

CPU_VCCST_PWRGD — R433 0R0402-PAD-2-GP — CPU_VCCST_PWRGD_R U2 → VCCST_PWRGD

H_PWRGD F8 → PROCPWRGD
PLTRST_CPU_N E7 → RESET#
PM_SYNC_CPU E8 → PM_SYNC
PM_DOWN_PCH — R422 20R2J-3-GP — PM_DOWN_CPU D8 → PM_DOWN
PECI_CPU G7 → PECI
THERMTRIP#_CPU_R D11 → THERMTRIP#

H_SKTOCC_N AB35 → SKTOCC#
SKL_CNL_N AB36 → PROC_SELECT#
CATERR#_CPU D13 → CATERR#

CFG0 H15 — R416 1KR2J-1-GP
CFG1 F15 — R418 1KR2J-1-GP
CFG2 F16 — R419 1KR2J-1-GP
CFG3 H16 — R420 1KR2J-1-GP
CFG4 F19 — R431 1KR2J-1-GP
CFG5 H18 — R429 1KR2J-1-GP
CFG6 G21 — R430 1KR2J-1-GP
CFG7 H20 — R417 1KR2J-1-GP
CFG8 G16 — R426 1KR2J-1-GP
CFG9 E16 — R433 1KR2J-1-GP
CFG10 F17 — R423 1KR2J-1-GP
CFG11 H17 — R428 1KR2J-1-GP
CFG12 G20 — R424 1KR2J-1-GP
CFG13 F20 — R425 1KR2J-1-GP
CFG14 F21 — R427 1KR2J-1-GP
CFG15 H19 — R458 1KR2J-1-GP

CFG16 E14 → SKL_PCUSTB_0_DN
CFG17 F14 → SKL_PCUSTB_0_DP
CFG18 G18 → SKL_PCUSTB_1_DN
CFG19 F18 → SKL_PCUSTB_1_DP

BPM#0 D16 → BPM_CPU_N0
BPM#1 D17 → BPM_CPU_N1
BPM#2 G14 → TP_CPU_G14
BPM#3 H14 → TP_CPU_H14

PROC_TDO H13 → H_TDO
PROC_TDI G12 → H_TDI
PROC_TMS F13 → H_TMS
PROC_TCK F11 → H_TCK

PROC_TRST# F12 → H_TRST_N
PROC_PREQ# B9 → H_PREQ_N
PROC_PRDY# B10 → H_PRDY_N

CFG_RCOMP M11 → CFG_RCOMP — R415 49D9R2F-GP

For CPU XDP

VCC_IO
SKL_CNL_N — R21 (R) 1KR2J-3-GP

1V_VCCST_VCCPLL_S3
VIDALERT#_VR1 — R470 56R2F-1-GP
VIDSOUT_VR1 — R471 100R2J-2-GP
PROCHOT#_R — R421 75R2F-2-GP

3D3V_S5
H_SKTOCC_N — R477 10KR2J-3-GP

H_TCK TERMINATION
PLACE NEAR CPU WITHIN 1.1 INCH
PLace Anywhere
H_TCK — R403 51R2J-2-GP
H_TRST_N — R407 (R) 51R2J-2-GP

- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]**: Reserved configuration lane.
- **CFG[4]**: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]**: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]**: Reserved configuration lanes.

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LOTES: 062.10015.0111

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Title: CPU_(THERMAL/CLOCK/PM/CFG)
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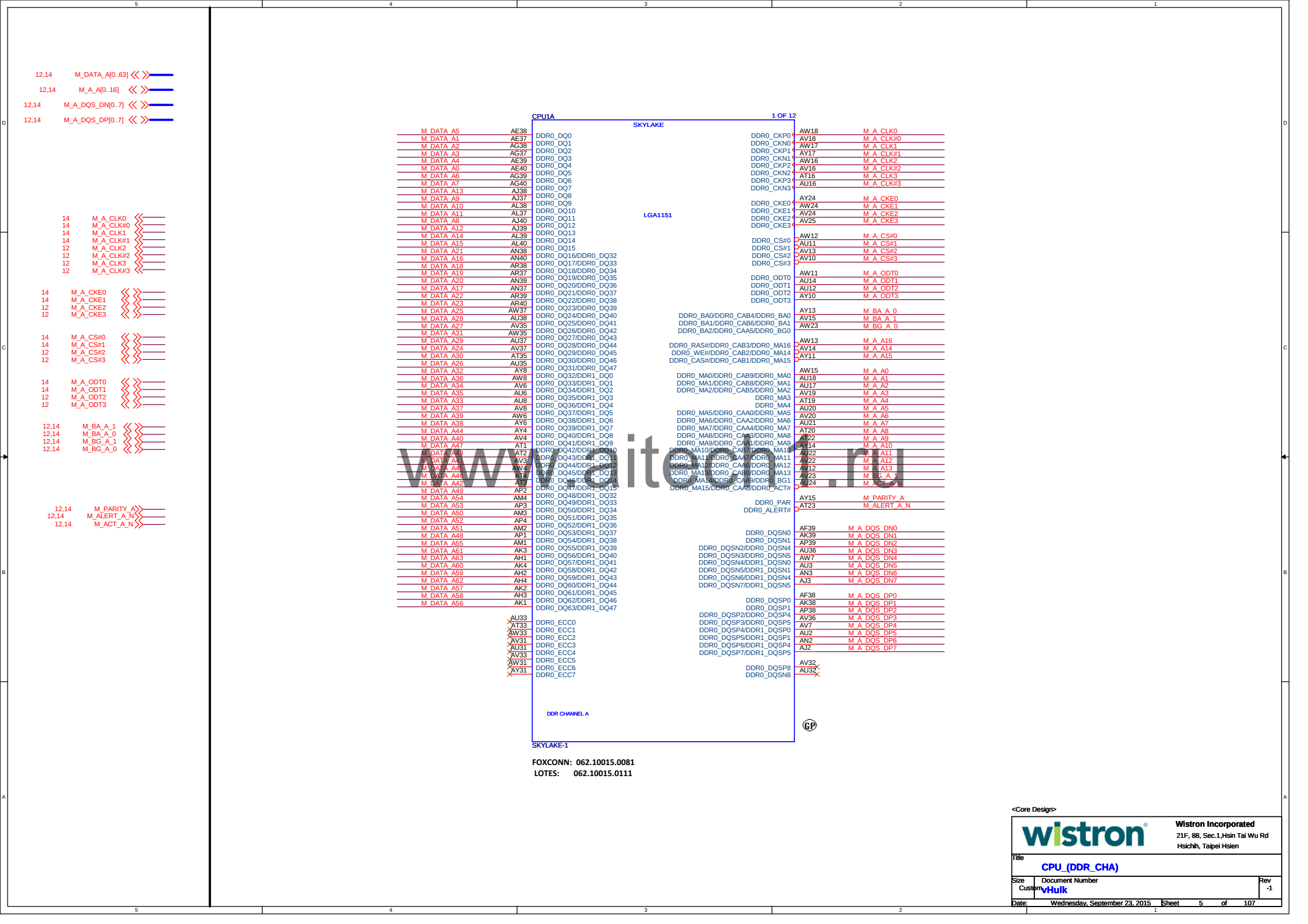
12,14 M_DATA_A[0..63]
12,14 M_A_A[0..16]
12,14 M_A_DQS_DN[0..7]
12,14 M_A_DQS_DP[0..7]
14 M_A_CLK0
14 M_A_CLK#0
14 M_A_CLK1
14 M_A_CLK#1
12 M_A_CLK2
12 M_A_CLK#2
12 M_A_CLK3
12 M_A_CLK#3
14 M_A_CKE0
14 M_A_CKE1
12 M_A_CKE2
12 M_A_CKE3
14 M_A_CS#0
14 M_A_CS#1
12 M_A_CS#2
12 M_A_CS#3
14 M_A_ODT0
14 M_A_ODT1
12 M_A_ODT2
12 M_A_ODT3
12,14 M_BA_A_1
12,14 M_BA_A_0
12,14 M_BG_A_1
12,14 M_BG_A_0
12,14 M_PARITY_A
12,14 M_ALERT_A_N
12,14 M_ACT_A_N
CPU1A
1 OF 12
SKYLAKE
LGA1151
DDR CHANNEL A
SKYLAKE-1
M_DATA_A5 AE38 DDR0_DQ0
M_DATA_A1 AE37 DDR0_DQ1
M_DATA_A2 AG38 DDR0_DQ2
M_DATA_A3 AG37 DDR0_DQ3
M_DATA_A4 AE39 DDR0_DQ4
M_DATA_A0 AE40 DDR0_DQ5
M_DATA_A6 AG39 DDR0_DQ6
M_DATA_A7 AG40 DDR0_DQ7
M_DATA_A13 AJ38 DDR0_DQ8
M_DATA_A9 AJ37 DDR0_DQ9
M_DATA_A10 AL38 DDR0_DQ10
M_DATA_A11 AL37 DDR0_DQ11
M_DATA_A8 AJ40 DDR0_DQ12
M_DATA_A12 AJ39 DDR0_DQ13
M_DATA_A14 AL39 DDR0_DQ14
M_DATA_A15 AL40 DDR0_DQ15
M_DATA_A21 AN38 DDR0_DQ16/DDR0_DQ32
M_DATA_A16 AN40 DDR0_DQ17/DDR0_DQ33
M_DATA_A18 AR38 DDR0_DQ18/DDR0_DQ34
M_DATA_A19 AR37 DDR0_DQ19/DDR0_DQ35
M_DATA_A20 AN39 DDR0_DQ20/DDR0_DQ36
M_DATA_A17 AN37 DDR0_DQ21/DDR0_DQ37
M_DATA_A22 AR39 DDR0_DQ22/DDR0_DQ38
M_DATA_A23 AR40 DDR0_DQ23/DDR0_DQ39
M_DATA_A25 AW37 DDR0_DQ24/DDR0_DQ40
M_DATA_A28 AU38 DDR0_DQ25/DDR0_DQ41
M_DATA_A27 AV35 DDR0_DQ26/DDR0_DQ42
M_DATA_A31 AW35 DDR0_DQ27/DDR0_DQ43
M_DATA_A29 AU37 DDR0_DQ28/DDR0_DQ44
M_DATA_A24 AV37 DDR0_DQ29/DDR0_DQ45
M_DATA_A30 AT35 DDR0_DQ30/DDR0_DQ46
M_DATA_A26 AU35 DDR0_DQ31/DDR0_DQ47
M_DATA_A32 AY8 DDR0_DQ32/DDR1_DQ0
M_DATA_A36 AW8 DDR0_DQ33/DDR1_DQ1
M_DATA_A34 AV6 DDR0_DQ34/DDR1_DQ2
M_DATA_A35 AU6 DDR0_DQ35/DDR1_DQ3
M_DATA_A33 AU8 DDR0_DQ36/DDR1_DQ4
M_DATA_A37 AV8 DDR0_DQ37/DDR1_DQ5
M_DATA_A39 AW6 DDR0_DQ38/DDR1_DQ6
M_DATA_A38 AY6 DDR0_DQ39/DDR1_DQ7
M_DATA_A44 AY4 DDR0_DQ40/DDR1_DQ8
M_DATA_A40 AV4 DDR0_DQ41/DDR1_DQ9
M_DATA_A47 AT1 DDR0_DQ42/DDR1_DQ10
M_DATA_A43 AT2 DDR0_DQ43/DDR1_DQ11
M_DATA_A41 AV3 DDR0_DQ44/DDR1_DQ12
M_DATA_A45 AW4 DDR0_DQ45/DDR1_DQ13
M_DATA_A46 AT4 DDR0_DQ46/DDR1_DQ14
M_DATA_A42 AT3 DDR0_DQ47/DDR1_DQ15
M_DATA_A49 AP2 DDR0_DQ48/DDR1_DQ32
M_DATA_A54 AM4 DDR0_DQ49/DDR1_DQ33
M_DATA_A53 AP3 DDR0_DQ50/DDR1_DQ34
M_DATA_A50 AM3 DDR0_DQ51/DDR1_DQ35
M_DATA_A52 AP4 DDR0_DQ52/DDR1_DQ36
M_DATA_A51 AM2 DDR0_DQ53/DDR1_DQ37
M_DATA_A48 AP1 DDR0_DQ54/DDR1_DQ38
M_DATA_A55 AM1 DDR0_DQ55/DDR1_DQ39
M_DATA_A61 AK3 DDR0_DQ56/DDR1_DQ40
M_DATA_A63 AH1 DDR0_DQ57/DDR1_DQ41
M_DATA_A60 AK4 DDR0_DQ58/DDR1_DQ42
M_DATA_A59 AH2 DDR0_DQ59/DDR1_DQ43
M_DATA_A62 AH4 DDR0_DQ60/DDR1_DQ44
M_DATA_A57 AK2 DDR0_DQ61/DDR1_DQ45
M_DATA_A58 AH3 DDR0_DQ62/DDR1_DQ46
M_DATA_A56 AK1 DDR0_DQ63/DDR1_DQ47
AU33 DDR0_ECC0
AT33 DDR0_ECC1
AW33 DDR0_ECC2
AV31 DDR0_ECC3
AU31 DDR0_ECC4
AV33 DDR0_ECC5
AW31 DDR0_ECC6
AY31 DDR0_ECC7
DDR0_CKP0 AW18 M_A_CLK0
DDR0_CKN0 AV18 M_A_CLK#0
DDR0_CKP1 AW17 M_A_CLK1
DDR0_CKN1 AY17 M_A_CLK#1
DDR0_CKP2 AW16 M_A_CLK2
DDR0_CKN2 AV16 M_A_CLK#2
DDR0_CKP3 AT16 M_A_CLK3
DDR0_CKN3 AU16 M_A_CLK#3
DDR0_CKE0 AY24 M_A_CKE0
DDR0_CKE1 AW24 M_A_CKE1
DDR0_CKE2 AV24 M_A_CKE2
DDR0_CKE3 AV25 M_A_CKE3
DDR0_CS#0 AW12 M_A_CS#0
DDR0_CS#1 AU11 M_A_CS#1
DDR0_CS#2 AV13 M_A_CS#2
DDR0_CS#3 AV10 M_A_CS#3
DDR0_ODT0 AW11 M_A_ODT0
DDR0_ODT1 AU14 M_A_ODT1
DDR0_ODT2 AU12 M_A_ODT2
DDR0_ODT3 AY10 M_A_ODT3
DDR0_BA0/DDR0_CAB4/DDR0_BA0 AY13 M_BA_A_0
DDR0_BA1/DDR0_CAB6/DDR0_BA1 AV15 M_BA_A_1
DDR0_BA2/DDR0_CAA5/DDR0_BG0 AW23 M_BG_A_0
DDR0_RAS#/DDR0_CAB3/DDR0_MA16 AW13 M_A_A16
DDR0_WE#/DDR0_CAB2/DDR0_MA14 AV14 M_A_A14
DDR0_CAS#/DDR0_CAB1/DDR0_MA15 AY11 M_A_A15
DDR0_MA0/DDR0_CAB9/DDR0_MA0 AW15 M_A_A0
DDR0_MA1/DDR0_CAB8/DDR0_MA1 AU18 M_A_A1
DDR0_MA2/DDR0_CAB5/DDR0_MA2 AU17 M_A_A2
DDR0_MA3 AV19 M_A_A3
DDR0_MA4 AT19 M_A_A4
DDR0_MA5/DDR0_CAA0/DDR0_MA5 AU20 M_A_A5
DDR0_MA6/DDR0_CAA2/DDR0_MA6 AV20 M_A_A6
DDR0_MA7/DDR0_CAA4/DDR0_MA7 AU21 M_A_A7
DDR0_MA8/DDR0_CAA3/DDR0_MA8 AT20 M_A_A8
DDR0_MA9/DDR0_CAA1/DDR0_MA9 AT22 M_A_A9
DDR0_MA10/DDR0_CAB7/DDR0_MA10 AY14 M_A_A10
DDR0_MA11/DDR0_CAA7/DDR0_MA11 AU22 M_A_A11
DDR0_MA12/DDR0_CAA6/DDR0_MA12 AV22 M_A_A12
DDR0_MA13/DDR0_CAB0/DDR0_MA13 AV12 M_A_A13
DDR0_MA17/DDR0_CAA9/DDR0_BG1 AV23 M_BG_A_1
DDR0_MA15/DDR0_CAA8/DDR0_ACT# AU24 M_ACT_A_N
DDR0_PAR AY15 M_PARITY_A
DDR0_ALERT# AT23 M_ALERT_A_N
DDR0_DQSN0 AF39 M_A_DQS_DN0
DDR0_DQSN1 AK39 M_A_DQS_DN1
DDR0_DQSN2/DDR0_DQSN4 AP39 M_A_DQS_DN2
DDR0_DQSN3/DDR0_DQSN5 AU36 M_A_DQS_DN3
DDR0_DQSN4/DDR1_DQSN0 AW7 M_A_DQS_DN4
DDR0_DQSN5/DDR1_DQSN1 AU3 M_A_DQS_DN5
DDR0_DQSN6/DDR1_DQSN4 AN3 M_A_DQS_DN6
DDR0_DQSN7/DDR1_DQSN5 AJ3 M_A_DQS_DN7
DDR0_DQSP0 AF38 M_A_DQS_DP0
DDR0_DQSP1 AK38 M_A_DQS_DP1
DDR0_DQSP2/DDR0_DQSP4 AP38 M_A_DQS_DP2
DDR0_DQSP3/DDR0_DQSP5 AV36 M_A_DQS_DP3
DDR0_DQSP4/DDR1_DQSP0 AV7 M_A_DQS_DP4
DDR0_DQSP5/DDR1_DQSP1 AU2 M_A_DQS_DP5
DDR0_DQSP6/DDR1_DQSP4 AN2 M_A_DQS_DP6
DDR0_DQSP7/DDR1_DQSP5 AJ2 M_A_DQS_DP7
DDR0_DQSP8 AV32
DDR0_DQSN8 AU32
GP
FOXCONN: 062.10015.0081
LOTES: 062.10015.0111
<Core Design>
wistron
Wistron Incorporated
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Hsichih, Taipei Hsien
Title
CPU_(DDR_CHA)
Size Custom
Document Number vHulk
Rev -1
Date: Wednesday, September 23, 2015
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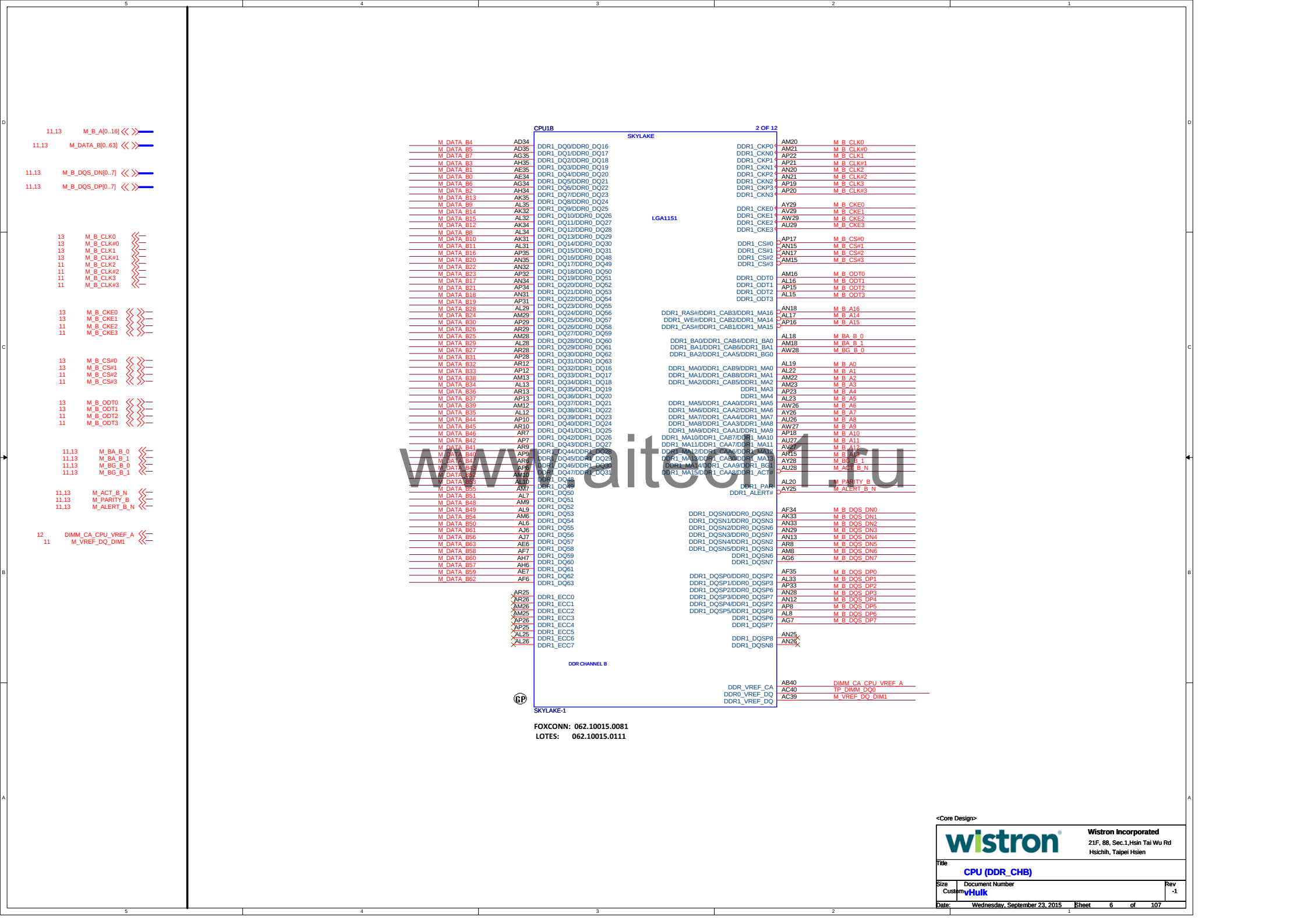

FOXCONN: 062.10015.0081
LOTES: 062.10015.0111

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Title: CPU (DDR_CHB)

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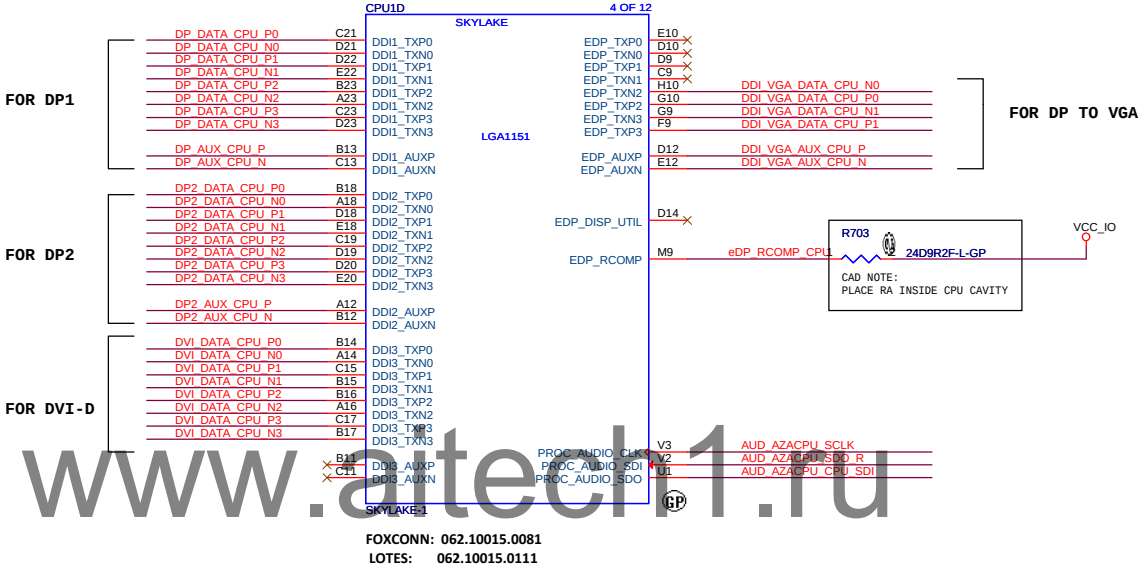
VBIOS set as DP

Note:
1. When using eDP bifurcation:
   - x2 eDP lanes for eDP panel (eDP_TXP[0:1], eDP_TXN[0:1])
   - x2 lanes for DP (eDP_TXP[2:3], eDP_TXN[2:3])



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FOXCONN: 062.10015.0081
LOTES: 062.10015.0111

<Core Design>

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Title: CPU (DDI/EDP)

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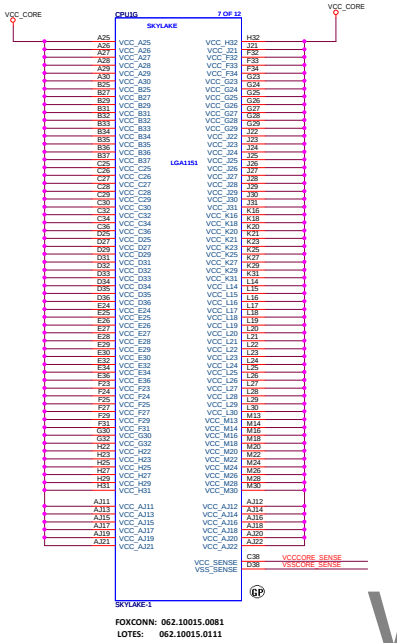
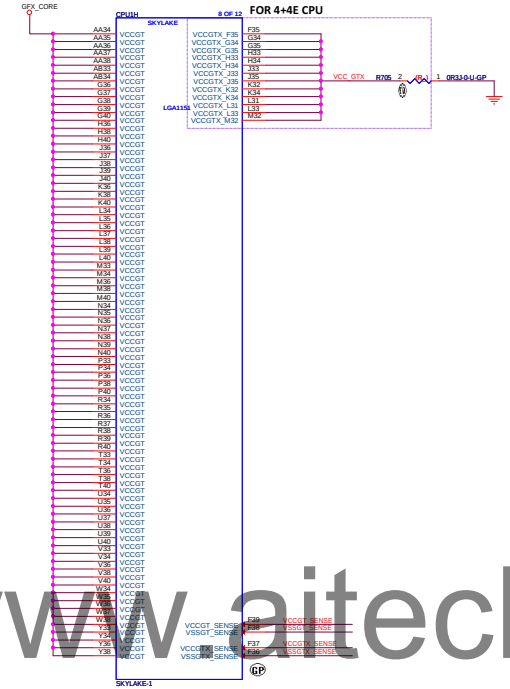
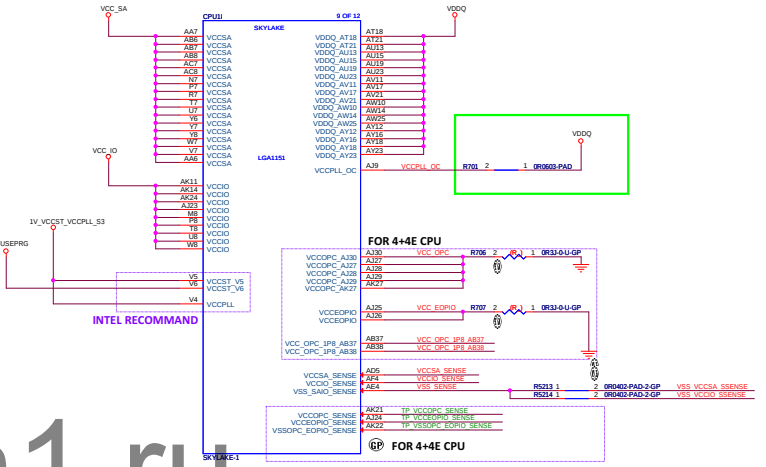
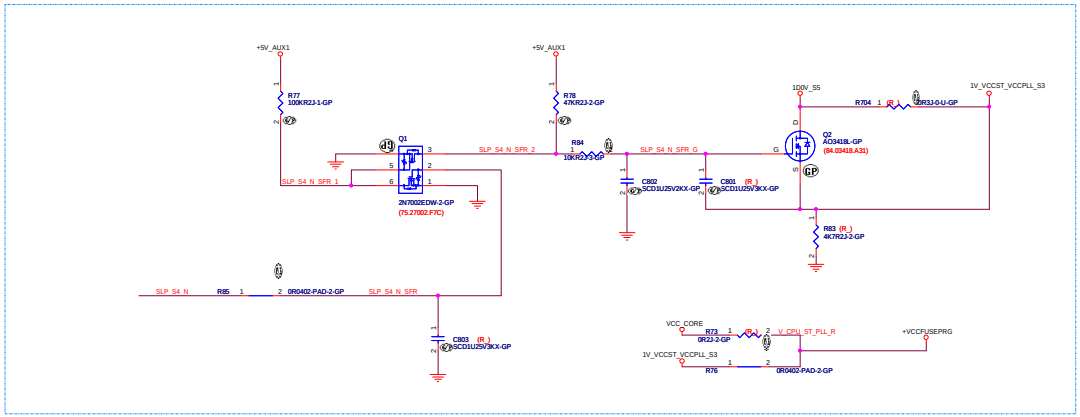
Greenlow Server Reference Circuit: Unused Power Pins Handling

Greenlow Server Reference board Zumba Beach does not support pGFX and EDRAM, hence some of the power rails such as VCCGT, VCCGTX, VCC_OPC_1P8, VCCOPC and VCCEOPIO are not required to be powered. Customers are recommended to reserve a 0 OHM 1/10W resistor between each power rail and GND. This provides the flexibility for the case where the validation results indicate the signals are good to be tied to GND or leave as unconnected. The final connection of these unused power rails will be updated in the Greenlow Server Platform Design Guide Rev 1.0 (IBP #541284, currently still at revision 0.75). Revision 1.0 is planned to be released around WW43.









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<Core Design>
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Title: CPU (CPU Power)
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Rev: -1
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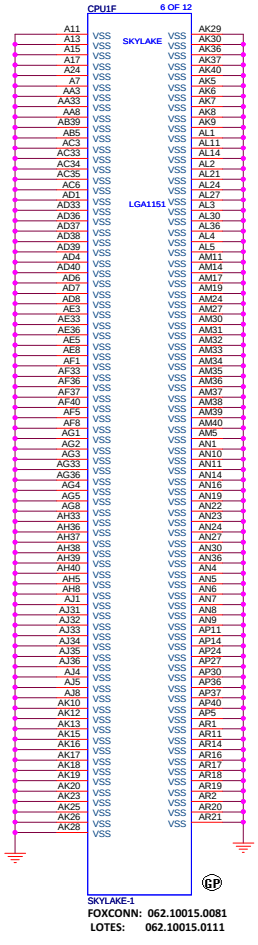
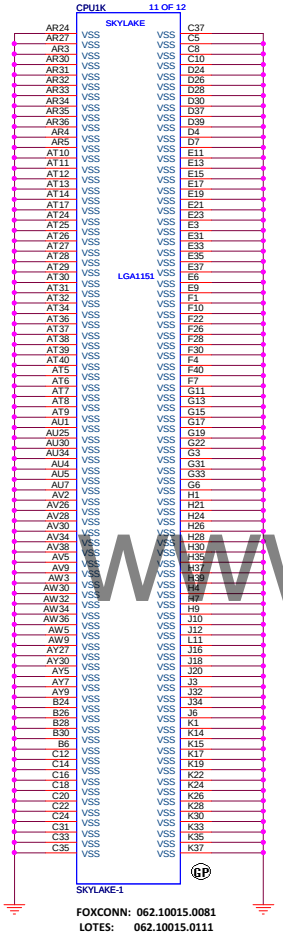
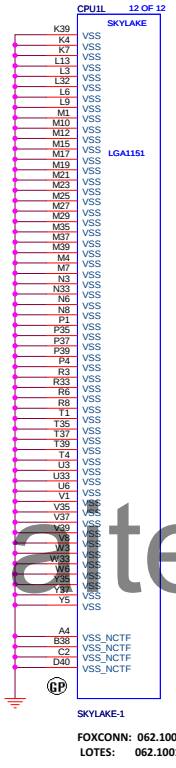
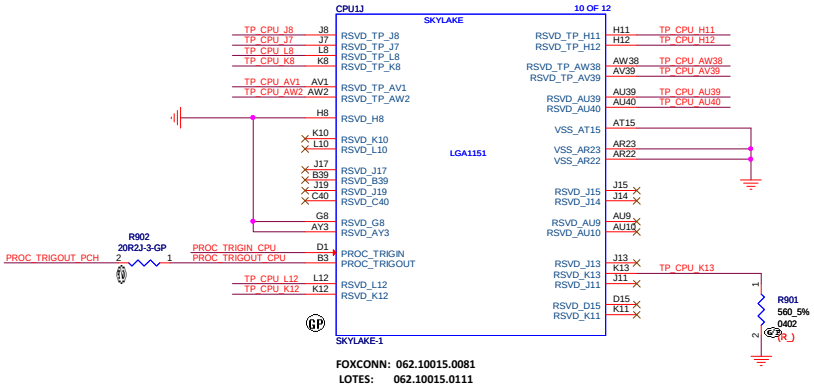
21 PROC_TRIGIN_CPU

21 PROC_TRIGOUT_PCH









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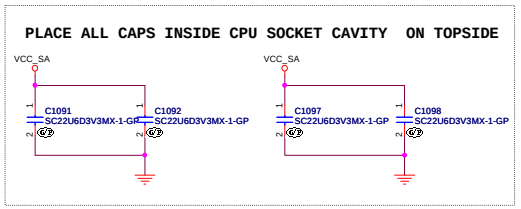
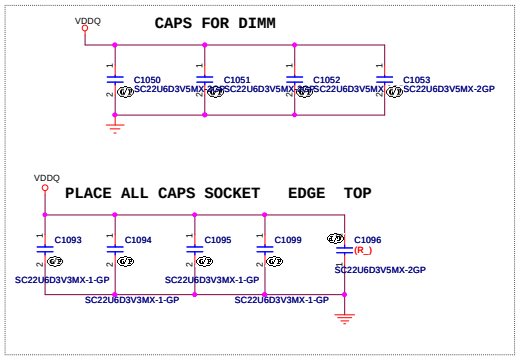
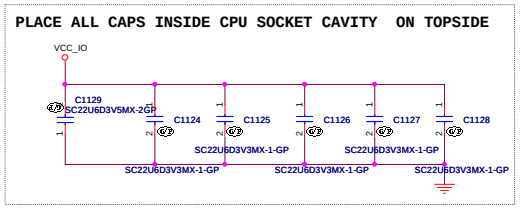
Title: CPU (VSS)

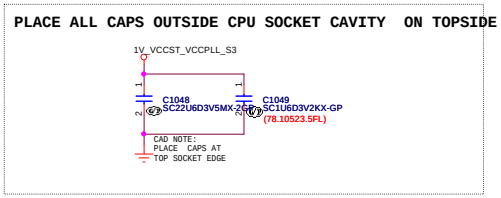
Size: C | Document Number: vHulk | Rev: -1

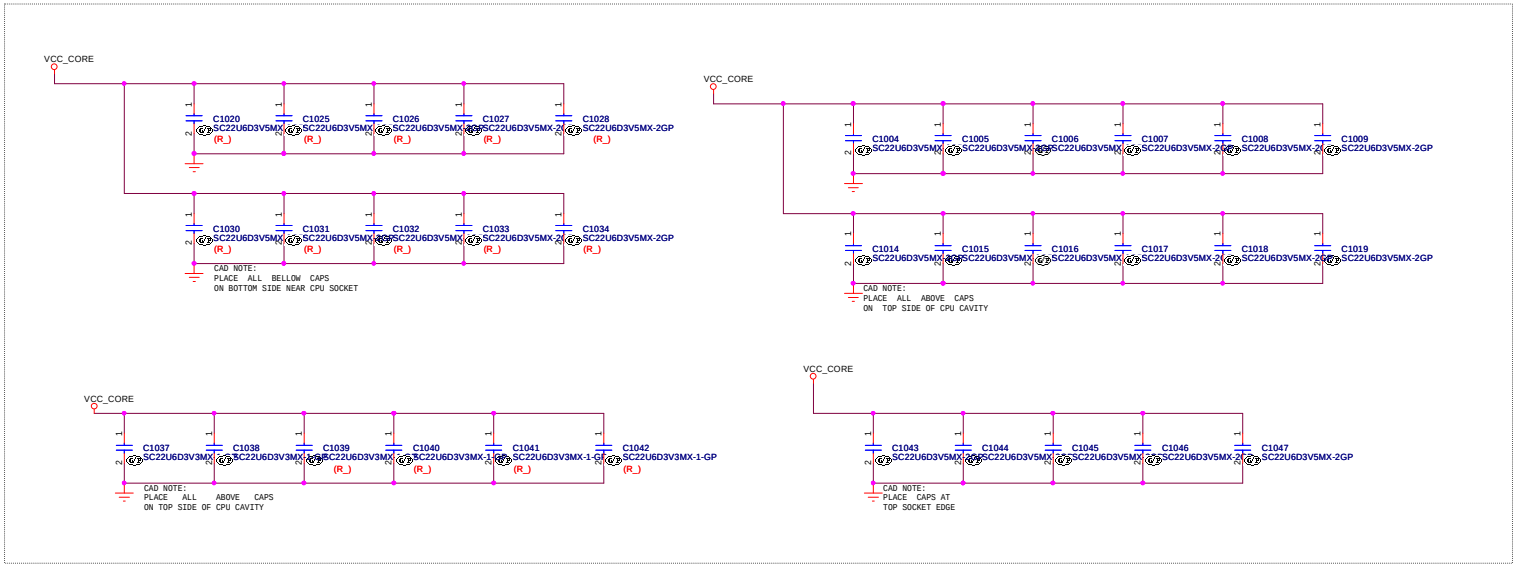
Date: Wednesday, September 23, 2015 | Sheet 9 of 107

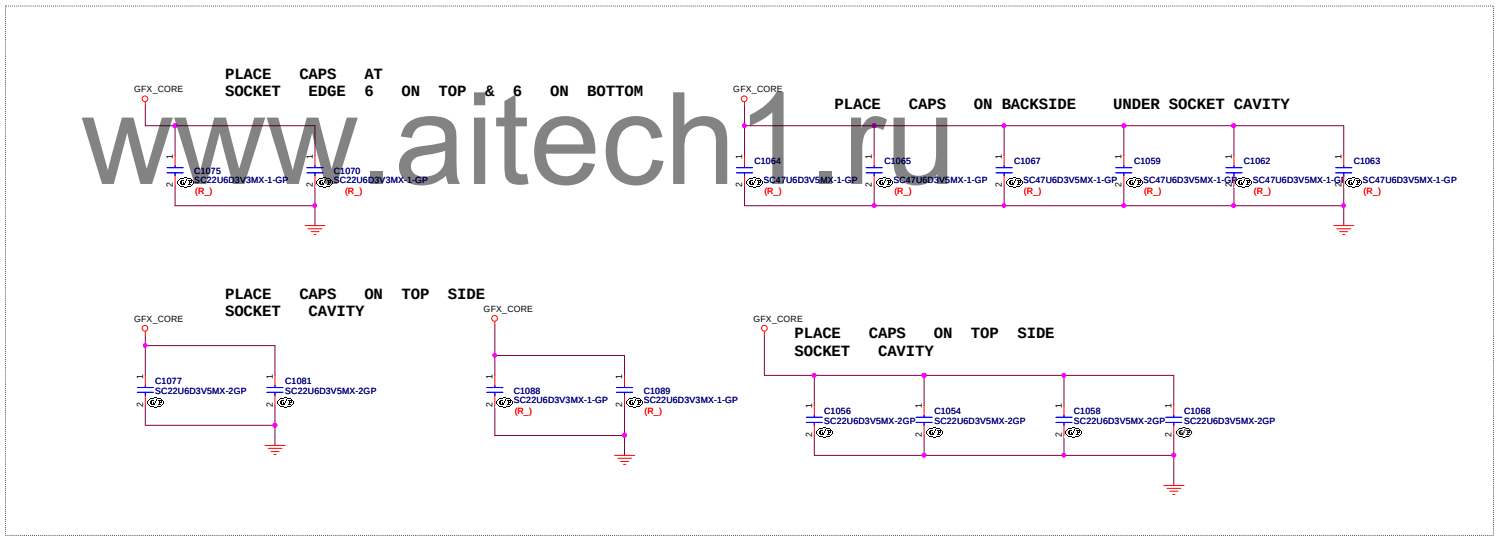












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<Core Design>

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Title: CPU Power CAP

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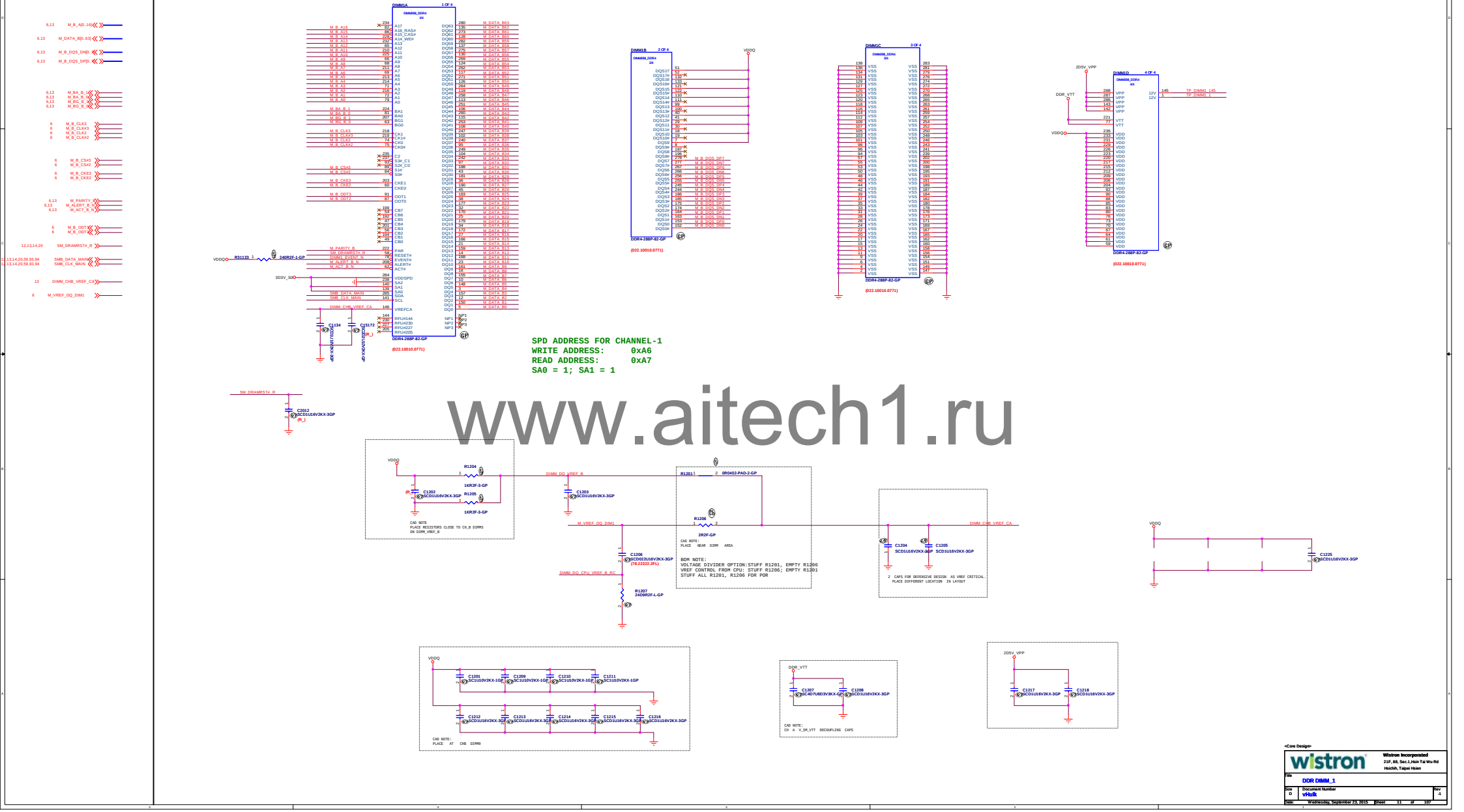
Date: Wednesday, September 23, 2015 | Sheet 10 of 107

CHANNEL B -- DIMM1



<Core Design>

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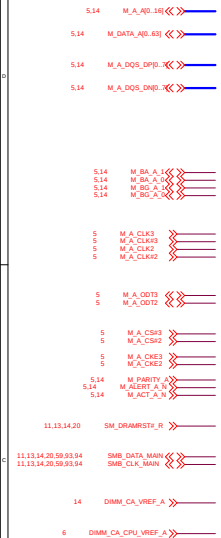
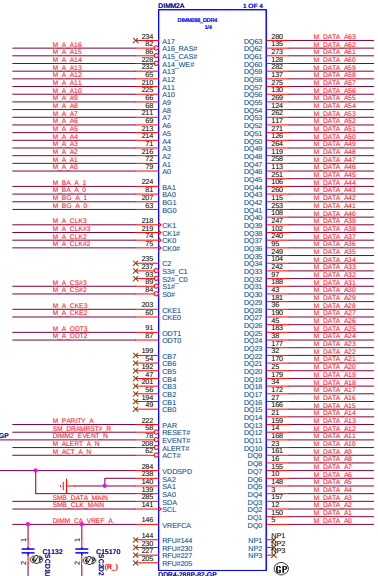
Title: DDR DIMM_1

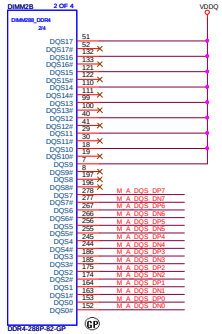
Size: D | Document Number: vHulk | Rev: -1

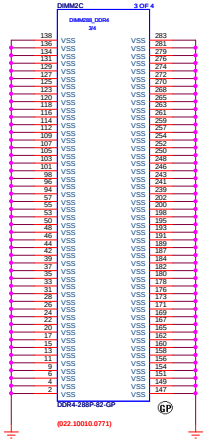
Date: Wednesday, September 23, 2015 | Sheet 11 of 107

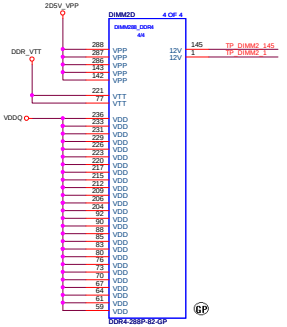
CHANNEL A -- DIMM1

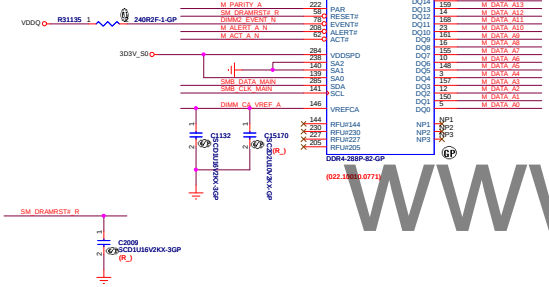












SPD ADDRESS FOR CHANNEL-1
WRITE ADDRESS: 0xA2
READ ADDRESS: 0xA3
SA0 = 1; SA1 = 0

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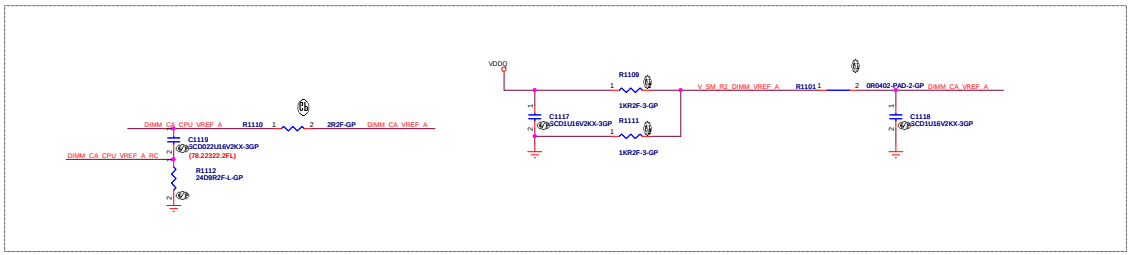

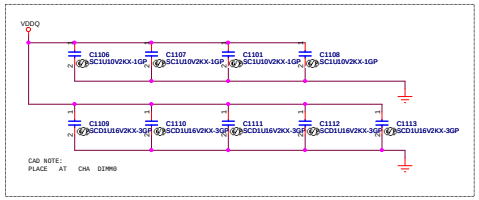

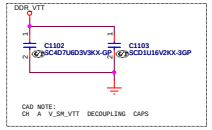

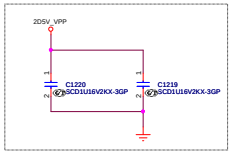

<Core Design>
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File: DDR-DIMM_2
Size: Document Number: Rev: -1
Custom: vHulk
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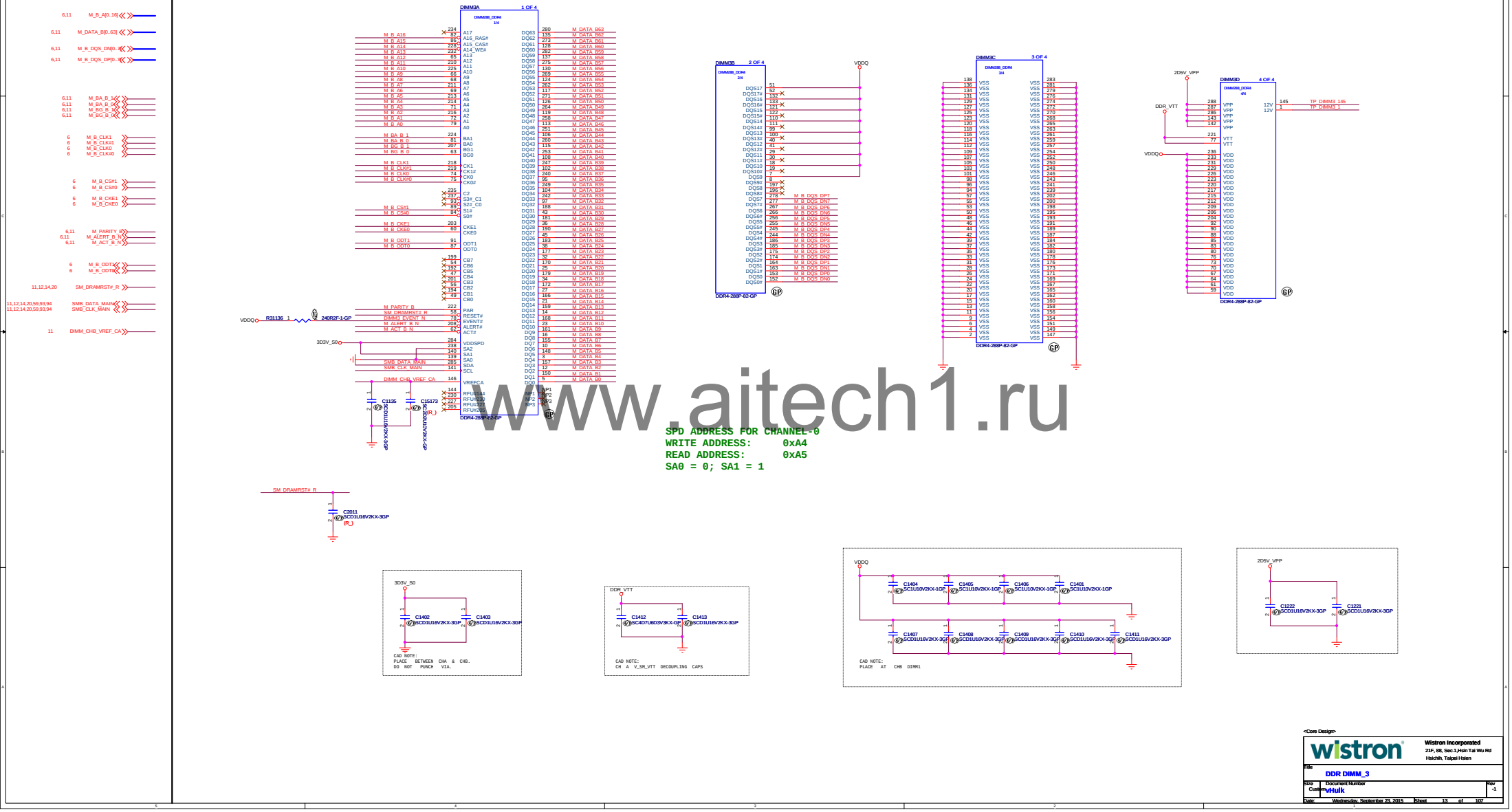
CHANNEL B -- DIMM0



SPD ADDRESS FOR CHANNEL-0
WRITE ADDRESS: 0xA4
READ ADDRESS: 0xA5
SA0 = 0; SA1 = 1

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File: DDR DIMM_3

Size: Custom | Document Number: vHulk | Rev: -1

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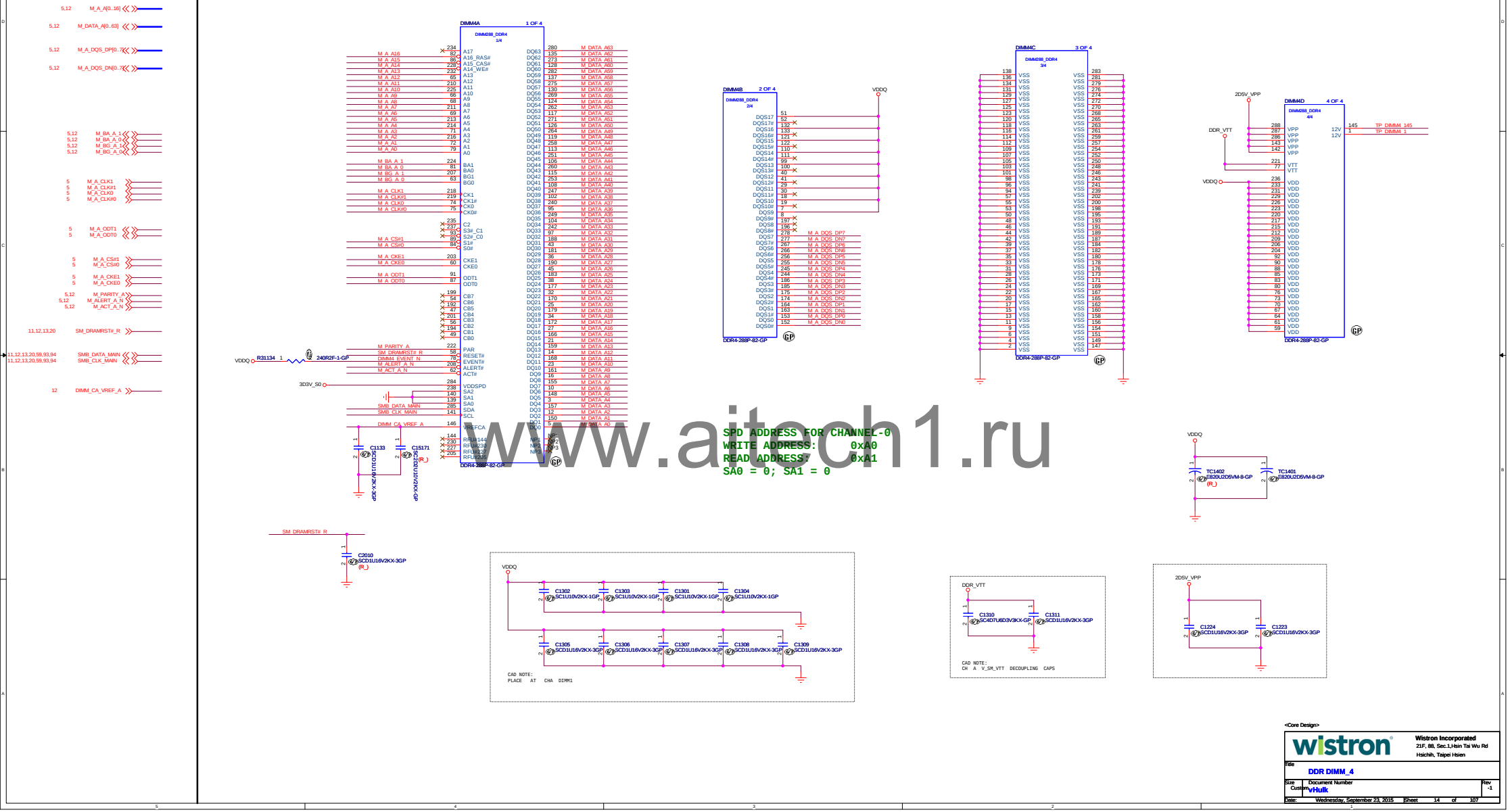
CHANNEL A -- DIMM0



SPD ADDRESS FOR CHANNEL-0
WRITE ADDRESS: 0xA0
READ ADDRESS : 0xA1
SA0 = 0; SA1 = 0

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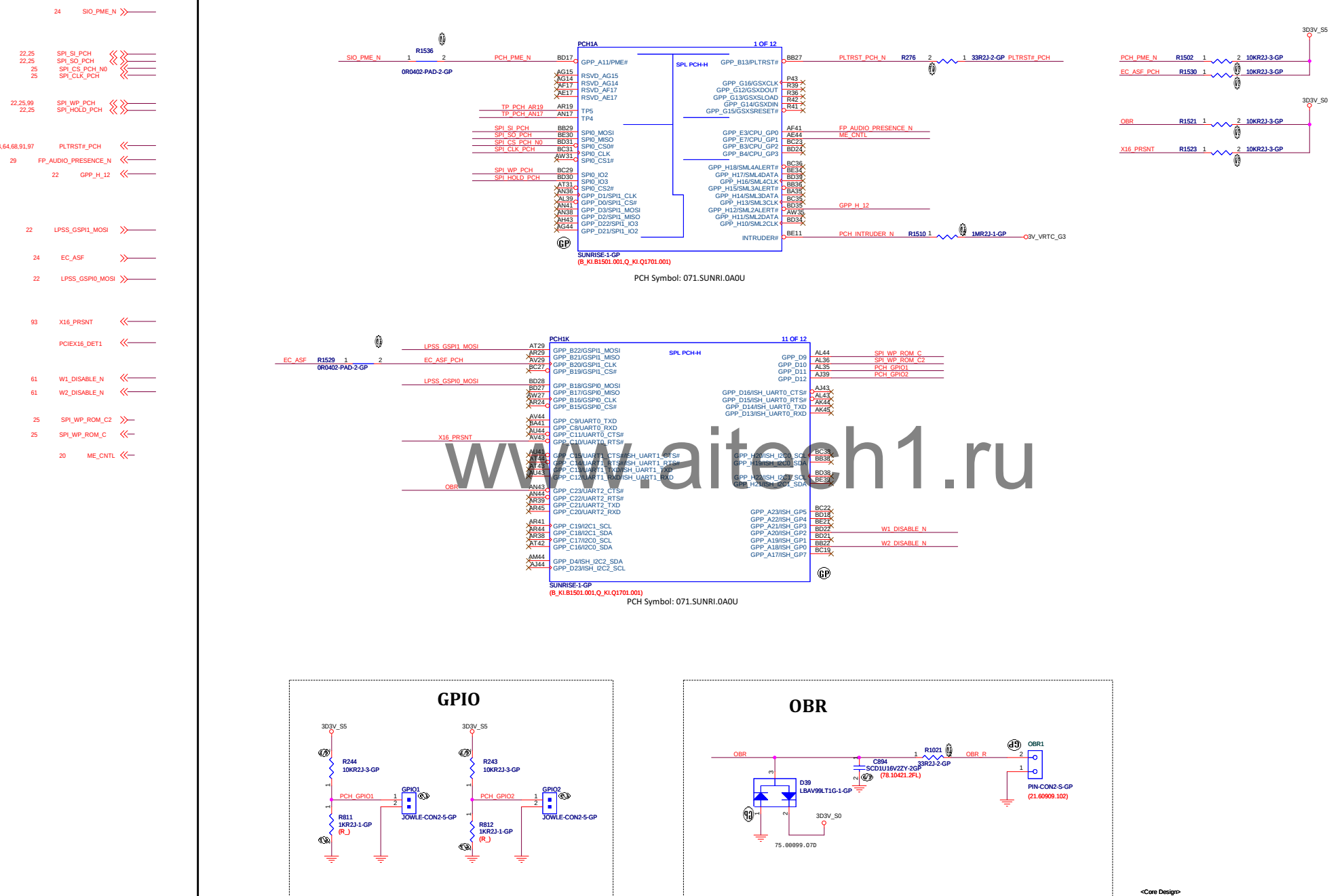
Title: DDR DIMM_4
Size: Custom | Document Number: vHulk | Rev: -1
Date: Wednesday, September 23, 2015 | Sheet 14 of 107



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GPIO

OBR

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Hsichih, Taipei Hsien

Title: PCH (SPI/UART/I2C)

Size	Document Number	Rev
C	vHulk	-1

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DMI

3 DMI_TX_CPU_N[0..3]
3 DMI_TX_CPU_P[0..3]
3 DMI_RX_CPU_N[0..3]
3 DMI_RX_CPU_P[0..3]

USB3.0

39 USB30_RX_PCH_N7
39 USB30_RX_PCH_P7
39 USB30_TX_PCH_N7
39 USB30_TX_PCH_P7
39 USB30_TX_PCH_N8
39 USB30_TX_PCH_P8
39 USB30_RX_PCH_N8
39 USB30_RX_PCH_P8

PCIE

31,97 PCIE_RX_LAN_N5
31,97 PCIE_RX_LAN_P5
31,97 PCIE_TX_LAN_N5
31,97 PCIE_TX_LAN_P5

61 PCIE_RX_PCH_N6
61 PCIE_RX_PCH_P6
61 PCIE_TX_CON_N6
61 PCIE_TX_CON_P6

59 PCIE_RX_PCH_N7
59 PCIE_RX_PCH_P7
59 PCIE_TX_CON_N7
59 PCIE_TX_CON_P7

94 PCIE_RX_PCH_N8
94 PCIE_RX_PCH_P8
94 PCIE_TX_CON_N8
94 PCIE_TX_CON_P8

USB2.0

38 USB_PCH_PN1
38 USB_PCH_PP1
38 USB_PCH_PN2
38 USB_PCH_PP2
38 USB_PCH_PN3
38 USB_PCH_PP3
38 USB_PCH_PN4
38 USB_PCH_PP4
39 USB_PCH_PN5
39 USB_PCH_PP5
39 USB_PCH_PN6
39 USB_PCH_PP6
37 USB_PCH_PN7
37 USB_PCH_PP7
37 USB_PCH_PN8
37 USB_PCH_PP8
37 USB_PCH_PN9
37 USB_PCH_PP9
36 USB_PCH_PN10
36 USB_PCH_PP10
36 USB_PCH_PN11
36 USB_PCH_PP11
61 USB_PCH_PN12
61 USB_PCH_PP12
39 USB_PCH_PN13
39 USB_PCH_PP13
39 USB_PCH_PN14
39 USB_PCH_PP14

USB OC CTRL

42 USB30_OC_H1#
42 USB30_OC_P1#
42 USB30_OC_P2#
22 VISACH2_D3
42 USB20_OC_P1#
42 USB20_OC_P2#

42 USB30_OC_H2#

DISPLAY CTRL

57 DP_HPD_PCH
56 DP2_HPD_PCH
55 DVI_DET_PCH
58 CRT_HPD_PCH

56 DP2_CTRLCLK_PCH
56 DP2_CTRLDATA_PCH
57 DP_CTRLCLK_PCH
57 DP_CTRLDATA_PCH
55 DVI_CLK_PCH
55 DVI_DATA_PCH

GPIO

4 H_SKTOCC_N

PCH1B 2 OF 12

SPL PCH-H

DMI_RXN0 L27 ← DMI_TX_CPU_N0
DMI_RXP0 N27 ← DMI_TX_CPU_P0
DMI_TXN0 C27 → DMI_RX_CPU_N0
DMI_TXP0 B27 → DMI_RX_CPU_P0
DMI_RXN1 E24 ← DMI_TX_CPU_N1
DMI_RXP1 G24 ← DMI_TX_CPU_P1
DMI_TXN1 B28 → DMI_RX_CPU_N1
DMI_TXP1 A28 → DMI_RX_CPU_P1
DMI_RXN2 G27 ← DMI_TX_CPU_N2
DMI_RXP2 E26 ← DMI_TX_CPU_P2
DMI_TXN2 B29 → DMI_RX_CPU_N2
DMI_TXP2 C29 → DMI_RX_CPU_P2
DMI_RXN3 L29 ← DMI_TX_CPU_N3
DMI_RXP3 K29 ← DMI_TX_CPU_P3
DMI_TXN3 B30 → DMI_RX_CPU_N3
DMI_TXP3 A30 → DMI_RX_CPU_P3

DMI

PEG_RCOMPN_CPU B18
PEG_RCOMPP_CPU C17
R1608 1 2 100R2F-L1-GP-U
PCIE_RCOMPN
PCIE_RCOMPP

USB30_RX_PCH_N7 H15
USB30_RX_PCH_P7 G15
USB30_TX_PCH_N7 A16
USB30_TX_PCH_P7 B16
USB30_TX_PCH_N8 B19
USB30_TX_PCH_P8 C19
USB30_RX_PCH_N8 E17
USB30_RX_PCH_P8 G17

PCIE1_RXN/USB3_7_RXN L17
PCIE1_RXP/USB3_7_RXP K17
PCIE1_TXN/USB3_7_TXN B20
PCIE1_TXP/USB3_7_TXP C20
PCIE2_TXN/USB3_8_TXN E20
PCIE2_TXP/USB3_8_TXP G19
PCIE2_RXN/USB3_8_RXN B21
PCIE2_RXP/USB3_8_RXP A21
PCIE3_RXN/USB3_9_RXN K19
PCIE3_RXP/USB3_9_RXP L19
PCIE3_TXN/USB3_9_TXN D22
PCIE3_TXP/USB3_9_TXP C22
PCIE4_RXN/USB3_10_RXN G22
PCIE4_RXP/USB3_10_RXP E22
PCIE4_TXN/USB3_10_TXN B22
PCIE4_TXP/USB3_10_TXP A23

PCIE5_RXN L22
PCIE5_RXP K22
PCIE5_TXN C23
PCIE5_TXP B23
PCIE6_RXN K24
PCIE6_RXP L24
PCIE6_TXN C24
PCIE6_TXP B24

PCH/USB3

USB 2.0

USB2N_1 AF5 USB_PCH_PN1
USB2P_1 AG7 USB_PCH_PP1
USB2N_2 AD5 USB_PCH_PN2
USB2P_2 AD7 USB_PCH_PP2
USB2N_3 AG8 USB_PCH_PN3
USB2P_3 AG10 USB_PCH_PP3
USB2N_4 AE1 USB_PCH_PN4
USB2P_4 AE2 USB_PCH_PP4
USB2N_5 AC2 USB_PCH_PN5
USB2P_5 AC3 USB_PCH_PP5
USB2N_6 AF2 USB_PCH_PN6
USB2P_6 AF3 USB_PCH_PP6
USB2N_7 AB3 USB_PCH_PN7
USB2P_7 AB2 USB_PCH_PP7
USB2N_8 AL8 USB_PCH_PN8
USB2P_8 AL7 USB_PCH_PP8
USB2N_9 AA1 USB_PCH_PN9
USB2P_9 AA2 USB_PCH_PP9
USB2N_10 AJ8 USB_PCH_PN10
USB2P_10 AJ7 USB_PCH_PP10
USB2N_11 W2 USB_PCH_PN11
USB2P_11 W3 USB_PCH_PP11
USB2N_12 AD3 USB_PCH_PN12
USB2P_12 AD2 USB_PCH_PP12
USB2N_13 V2 USB_PCH_PN13
USB2P_13 V1 USB_PCH_PP13
USB2N_14 AJ11 USB_PCH_PN14
USB2P_14 AJ13 USB_PCH_PP14

GPP_E9/USB2_OC0# AD43 USB30_OC_H1#
GPP_E10/USB2_OC1# AD42 USB30_OC_P1#
GPP_E11/USB2_OC2# AD39 USB30_OC_P2#
GPP_E12/USB2_OC3# AC44 VISACH2_D3
GPP_F15/USB2_OCB_4 Y43 USB20_OC_P1#
GPP_F16/USB2_OCB_5 Y41 USB20_OC_P2#
GPP_F17/USB2_OCB_6 W44 USB20_OC_C1#
GPP_F18/USB2_OCB_7 W43 USB30_OC_H2#

USB 3.0 OC
USB 2.0 OC

3D3V_S5
USB20_OC_C1# R1620 1 2 10KR2J-3-GP

USB2_COMP AG3 USB2_COMP R1604 1 2 113R2F-GP
USB2_VBUSSENSE AD10 USB2_VBUSSENSE R1605 1 2 1KR2J-1-GP
RSVD_AB13 AB13 RSVD_AB13
USB2_ID AG2 USB2_ID R1606 1 2 1KR2J-1-GP

GPD7/RSVD BD14 TP_PCH_BD14

SUNRISE-1-GP
(B_KI.B1501.001,Q_KI.Q1701.001)

PCH Symbol: 071.SUNRI.0A0U

Close to CONN

FOR LAN
FOR NGFFE1
PCIE TO PCI Bridge
FOR PCIE2

PCIE_TX_LAN_N5 C1608 1 2 SCD1U16V2KX-3GP → PCIE_RX_LAN_N5
PCIE_TX_LAN_P5 C1603 1 2 SCD1U16V2KX-3GP → PCIE_RX_LAN_P5
PCIE_TX_CON_N6 C1614 1 2 SCD22U10V2KX-1GP → PCIE_RX_PCH_N6
PCIE_TX_CON_P6 C1613 1 2 SCD22U10V2KX-1GP → PCIE_RX_PCH_P6
PCIE_TX_CON_N7 C1616 1 2 SCD1U16V2KX-3GP → PCIE_RX_PCH_N7
PCIE_TX_CON_P7 C1615 1 2 SCD1U16V2KX-3GP → PCIE_RX_PCH_P7
PCIE_TX_CON_N8 C1617 1 2 SCD22U10V2KX-1GP → PCIE_RX_PCH_N8
PCIE_TX_CON_P8 C1618 1 2 SCD22U10V2KX-1GP → PCIE_RX_PCH_P8

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USB Table

Pair	Device
1	USB3.0 Ext. port 1 (Rear)
2	USB3.0 Ext. port 2 (Rear)
3	USB3.0 Ext. port 3 (Rear)
4	USB3.0 Ext. port 4 (Rear)
5	USB3.0 Ext. Header (Front)
6	USB3.0 Ext. Header (Front)
7	USB2.0 Ext. Header (Front)
8	CR Ext. Header (Front)
9	USB2.0 Ext. Header (Front)
10	RJ45+USB Dual port
11	RJ45+USB Dual port
12	NGFFE1
13	USB3.0 Ext.Header (Front) for Q170 bom option
14	USB3.0 Ext.Header (Front) for Q170 bom option

PORT7 - USB30
FRONT HEADER 2
PORT8 - USB30
FRONT HEADER 2

BOARD ID

3D3V_S5
(R_) R1601 10KR2J-3-GP BOARD_ID_2 R1619 10KR2J-3-GP
(R_) R1616 10KR2J-3-GP BOARD_ID_1 R1615 10KR2J-3-GP
(Q_) R1618 10KR2J-3-GP BOARD_ID_0 R1617 10KR2J-3-GP (B_)

Board_ID_0
pull high for Q170
pull low for B150

2014/9/9
DDI1 TO DP1
DDI2 TO DP2
DDI3 TO DVI

PCH1E 5 OF 12

SPL PCH-H

DP_HPD_PCH AW4
DP2_HPD_PCH AY2
DVI_DET_PCH AV4
R1702 2 1 0R0402-PAD-2-GP DDPE_HPD BA4

GPP_I0/DDPB_HPD0
GPP_I1/DDPC_HPD1
GPP_I2/DDPD_HPD2
GPP_I3/DDPE_HPD3

GPP_I7/DDPC_CTRLCLK BB3 DP2_CTRLCLK_PCH
GPP_I8/DDPC_CTRLDATA BD6 DP2_CTRLDATA_PCH
GPP_I5/DDPB_CTRLCLK BA5 DP_CTRLCLK_PCH
GPP_I6/DDPB_CTRLDATA BC4 DP_CTRLDATA_PCH
GPP_I9/DDPD_CTRLCLK BE5 DVI_CLK_PCH
GPP_I10/DDPD_CTRLDATA BE6 DVI_DATA_PCH

GPP_F14 Y44 H_SKTOCC_N
GPP_F23 V44
GPP_F22 W39

GPP_G23 L43 BOARD_ID_2
GPP_G22 L44 BOARD_ID_1
GPP_G21 U35 BOARD_ID_0
GPP_G20 R35
GPP_H23 BD38

CRT_HPD_PCH → R1707 2 1 (R_) 0R2J-2-GP EDP_HPD BD7 GPP_I4/EDP_HPD
R9703 100KR2J-1-GP

SUNRISE-1-GP
(B_KI.B1501.001,Q_KI.Q1701.001)

PCH Symbol: 071.SUNRI.0A0U

<Core Design>

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: PCH (DMI/PCI-E/USB)
Size: C
Document Number: vHulk
Rev: -1
Date: Wednesday, September 23, 2015
Sheet 16 of 107

CL BUS

61	WLAN_CLK_PCH
61	WLAN_DAT_PCH
61	WLAN_RST_PCH

PCIE

94	PCIE_TX_CON_P11
94	PCIE_TX_CON_N11
94	PCIE_RX_PCH_P11
94	PCIE_RX_PCH_N11

SATA PORT

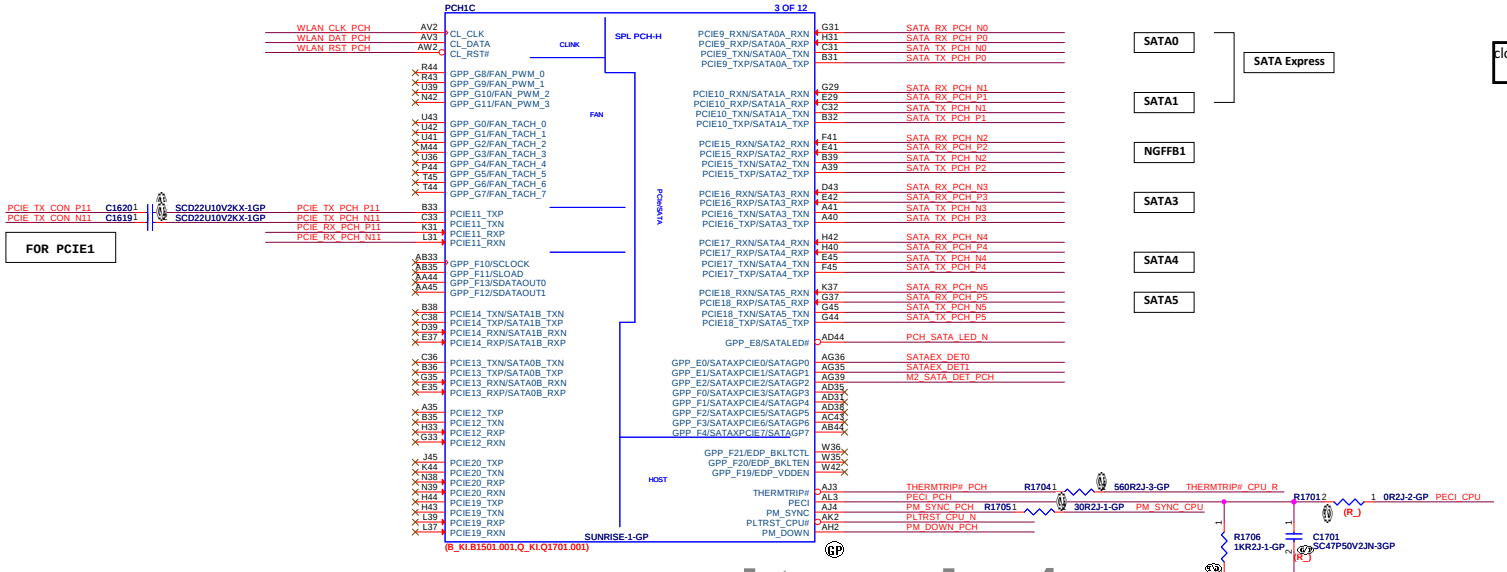
60	SATA_RX_PCH_N0
60	SATA_RX_PCH_P0
60	SATA_TX_PCH_N0
60	SATA_TX_PCH_P0
60	SATA_RX_PCH_N1
60	SATA_RX_PCH_P1
60	SATA_TX_PCH_N1
60	SATA_TX_PCH_P1
63	SATA_RX_PCH_N2
63	SATA_RX_PCH_P2
63	SATA_TX_PCH_N2
63	SATA_TX_PCH_P2
60	SATA_RX_PCH_N3
60	SATA_RX_PCH_P3
60	SATA_TX_PCH_N3
60	SATA_TX_PCH_P3
60	SATA_RX_PCH_N4
60	SATA_RX_PCH_P4
60	SATA_TX_PCH_N4
60	SATA_TX_PCH_P4
60	SATA_RX_PCH_N5
60	SATA_RX_PCH_P5
60	SATA_TX_PCH_N5
60	SATA_TX_PCH_P5

SATA DET

60	SATAEX_DET0
60	SATAEX_DET1
63	M2_SATA_DET_PCH
64	PCH_SATA_LED_N

HOST

4	THERMTRIP#_CPU_R
4,24	PECI_CPU
4	PLTRST_CPU_N
4	PM_DOWN_PCH
4	PM_SYNC_CPU



PCH Symbol: 071.SUNRI.0A0U

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Hsichih, Taipei Hsien

Title: PCH (PCI-E/SATA)

Size: Custom | Document Number: vHulk | Rev: -1

Date: Wednesday, September 23, 2015 | Sheet 17 of 107

CPU CLK

4	CPU_CLK24M_PCH
4	CPU_CLK24M_PCH#
4	CPU_BCLK_PCH
4	CPU_BCLK_PCH#

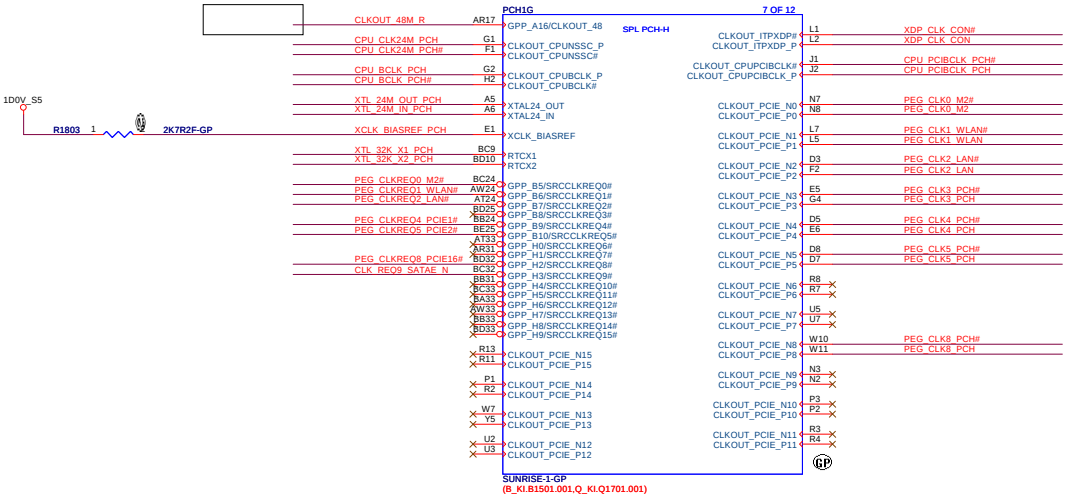
CLKREQ

63	PEG_CLKREQ0_M2#
61	PEG_CLKREQ1_WLAN#
31,97	PEG_CLKREQ2_LAN#
60	CLK_REQ9_SATAE_N
94	PEG_CLKREQ4_PCIE1#
94	PEG_CLKREQ5_PCIE2#
93	PEG_CLKREQ8_PCIE16#

CLOCK

	XDP_CLK_CON#
	XDP_CLK_CON
4	CPU_PCIBCLK_PCH#
4	CPU_PCIBCLK_PCH
63	PEG_CLK0_M2#
63	PEG_CLK0_M2
61	PEG_CLK1_WLAN#
61	PEG_CLK1_WLAN
31,97	PEG_CLK2_LAN#
31,97	PEG_CLK2_LAN
59	PEG_CLK3_PCH#
59	PEG_CLK3_PCH
94	PEG_CLK4_PCH#
94	PEG_CLK4_PCH
94	PEG_CLK5_PCH#
94	PEG_CLK5_PCH
93	PEG_CLK8_PCH#
93	PEG_CLK8_PCH

CLKOUT_48 is only supported and enabled on SKL-H Server



PCH Symbol: 071.SUNRI.0A0U

CLK OUT for CPU XDP

NGFFB1 (SSD)

NGFFE1 (WLAN)

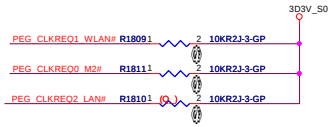
INTEL & REALTK LAN

FOR PCIE to PCI bridge

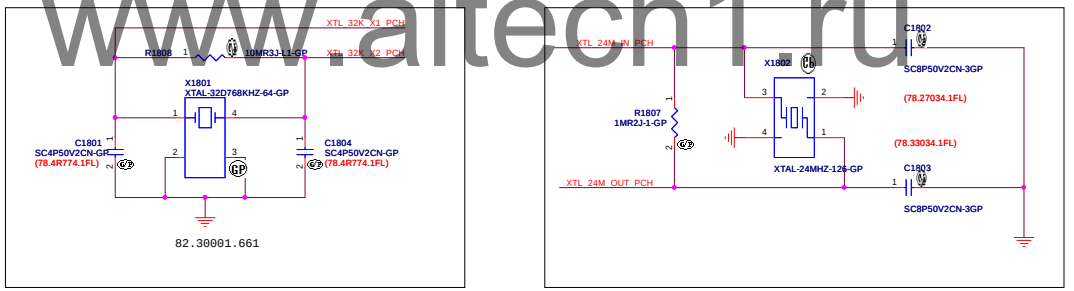
FOR PCIE1 CONN

FOR PCIE2 CONN

FOR PCIEx16 CONN



RTC CLOCK



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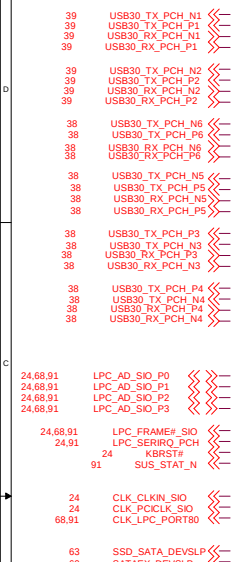
Hsichih, Taipei Hsien

Title: PCH(CLOCK/CL)

Size: Custom | Document Number: vHulk | Rev: -1

Date: Wednesday, September 23, 2015 | Sheet 18 of 107



PORT1 - USB30 FRONT HEADER 1

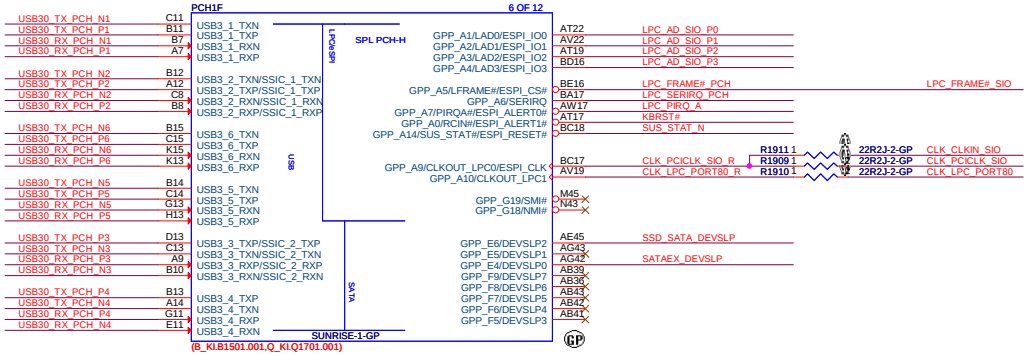
PORT2 - USB30 FRONT HEADER 1

PORT6 - USB30 REAR PORT

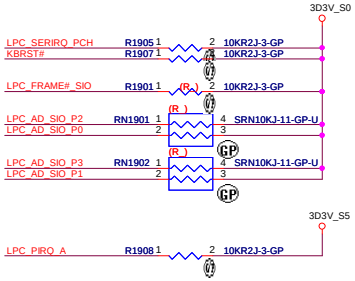
PORT5 - USB30 REAR PORT

PORT3 - USB30 REAR PORT

PORT4 - USB30 REAR PORT

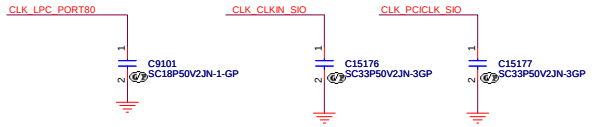


PCH Symbol: 071.SUNRI.0A0U



Integrated Pull-ups and Pull-downs

Signal	Resistor Type	Value	Notes
LAD[3:0]	Pull-up	15 - 40 KΩ	



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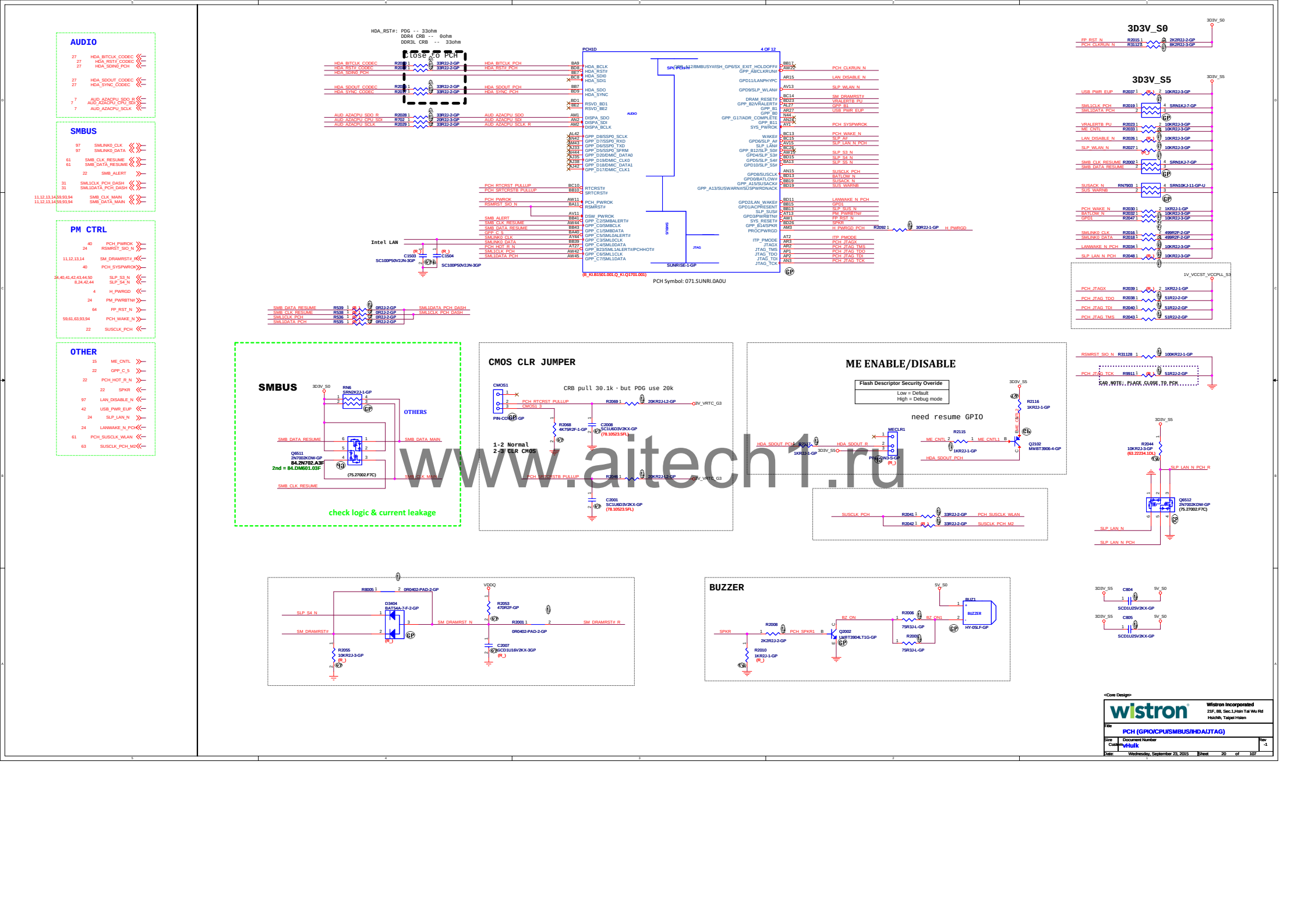
Title: PCH (USB/ESPI)

Size: Custom | Document Number: vHulk | Rev: -1

Date: Wednesday, September 23, 2015 | Sheet 19 of 107


AUDIO
HDA_BITCLK_CODEC
HDA_RST#_CODEC
HDA_SDIN0_PCH
HDA_SDOUT_CODEC
HDA_SYNC_CODEC
AUD_AZACPU_SDO_R
AUD_AZACPU_CPU_SDI
AUD_AZACPU_SCLK
SMBUS
SMLINK0_CLK
SMLINK0_DATA
SMB_CLK_RESUME
SMB_DATA_RESUME
SMB_ALERT
SML1CLK_PCH_DASH
SML1DATA_PCH_DASH
SMB_CLK_MAIN
SMB_DATA_MAIN
PM_CTRL
PCH_PWROK
RSMRST_SIO_N
SM_DRAMRST#_R
PCH_SYSPWROK
SLP_S3_N
SLP_S4_N
H_PWRGD
PM_PWRBTN#
FP_RST_N
PCH_WAKE_N
SUSCLK_PCH
OTHER
ME_CNTL
GPP_C_5
PCH_HOT_R_N
SPKR
LAN_DISABLE_N
USB_PWR_EUP
SLP_LAN_N
LANWAKE_N_PCH
PCH_SUSCLK_WLAN
SUSCLK_PCH_M2
HDA_RST#: PDG -- 33ohm
DDR4 CRB -- 0ohm
DDR3L CRB -- 33ohm
CLOSE TO PCH
Intel LAN
PCH1D
4 OF 12
PCH Symbol: 071.SUNRI.0A0U
3D3V_S0
3D3V_S5
1V_VCCST_VCCPLL_S3
SMBUS
check logic & current leakage
CMOS CLR JUMPER
CRB pull 30.1k , but PDG use 20k
1-2 Normal
2-3 CLR CMOS
ME ENABLE/DISABLE
Flash Descriptor Security Overide
Low = Default
High = Debug mode
need resume GPIO
CAN NOTE: PLACE CLOSE TO PCH
BUZZER
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Hsichih, Taipei Hsien
PCH (GPIO/CPU/SMBUS/IHDA/JTAG)
vHulk
Wednesday, September 23, 2015
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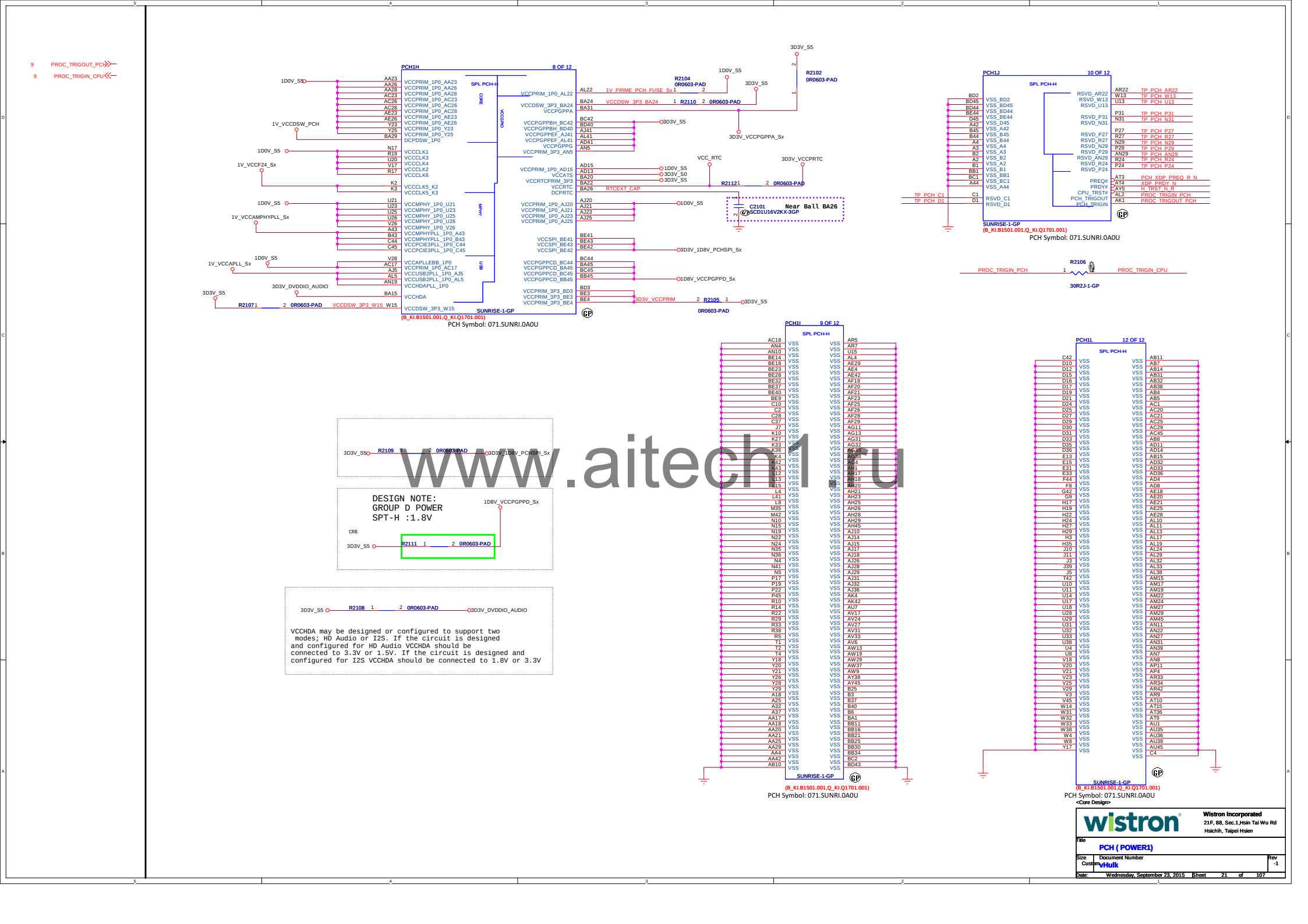

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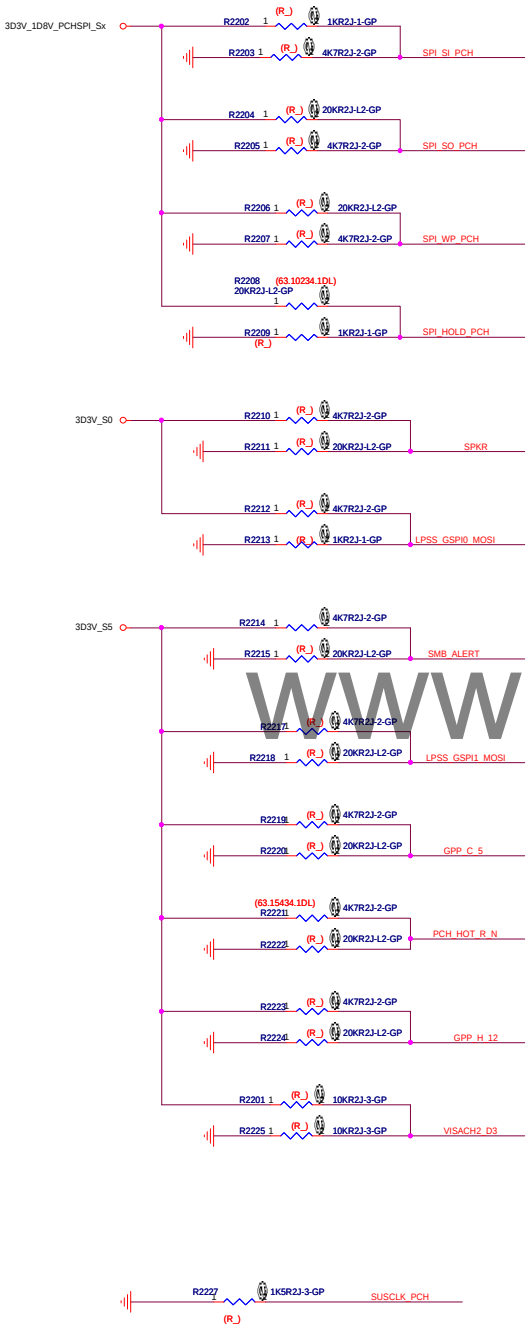
15,25 SPI_SI_PCH
15,25 SPI_SO_PCH
15,25,99 SPI_WP_PCH
15,25 SPI_HOLD_PCH
20 SPKR
15 LPSS_GSPI0_MOSI
20 SMB_ALERT
15 LPSS_GSPI1_MOSI
20 SUSCLK_PCH
20 GPP_C_5
20 PCH_HOT_R_N
15 GPP_H_12
16 VISACH2_D3



PCH STRAP FUNCTIONS

SPI_SI_PCH (SPI0_MOSI)	0: Enable boot halt 1: Disable boot halt The internal PU resistor is enabled when RSMRST# is asserted and is switched to the internal PD when RSMRST# is de-asserted.
SPI_SO_PCH (SPI0_MISO)	0: Disable JTAG ODT 1: Enable JTAG ODT The internal PU resistor is enabled when RSMRST# is asserted
SPI_WP_PCH (SPI0_IO2)	0: Enable consent strap 1: Disable consent strap PCH has internal weak PU
SPI_HOLD_PCH (SPI0_IO3)	0: Enable personality strap 1: Disable personality strap PCH has internal weak PU

SPKR (SPKR / GPP_B14)	0: Disable Top Swap mode. (Default) 1: Enable Top Swap mode. PCH internal pull-down is disabled after PLTRST# deasserts.
LPSS_GSPI0_MOSI (GPP_B18/GSPI0_MOSI)	0: Disable No Reboot mode. 1: Enable No Reboot mode This function is useful when running ITP/XDP. The internal pull-down is disabled after PLTRST# deasserts.
SMB_ALERT (GPP_C2/SMBALERT#)	0: Disable TSL confidentiality 1: Enable TSL confidentiality (default) The internal pull-down is disabled after RSMRST# deasserts.
LPSS_GSPI1_MOSI (GPP_B22/GSPI1_MOSI)	BOOT SELECT STRAP 0: SPI select 1: LPC select The internal pull-down is disabled after PLTRST# deasserts.
GPP_C_5 (GPP_C5/SML0ALERT#)	ESPI/LPC SELECT STRAP 0: LPC is selected for EC. 1: eSPI is selected for EC. The internal pull-down is disabled after RSMRST# deasserts.
PCH_HOT_R_N (GPP_B23/SML1ALERT#/PCHHOT#)	0: Disable Exi boot stall bypass 1: Enable Exi boot stall bypass The internal PD resistor is disable after RSMRST# de-asserted.
GPP_H_12 (GPP_H12/SML2ALERT#)	ESPI flash sharing mode 0: Master attached flash sharing 1: Slave attached flash sharing PCH has internal weak PD.
VISACH2_D3 (GPP_E12)	DFX test mode 0: XTAL input is single ended. 1: XTAL input is differential. The internal PD resistoris disabled after RSMRST# de-asserts
HDA_SDOUT_PCH (HDA_SDO)	0: Enable security measures defined in the Flash Descriptor. 1: Disable Flash Descriptor Security (override). The internal pull-down is disabled after PLTRST# deasserts.
SUSCLK_PCH (GPD8/SUSCLK)	0: Disable OD PLL VR 1: Enable OD PLL VR

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<Core Design>

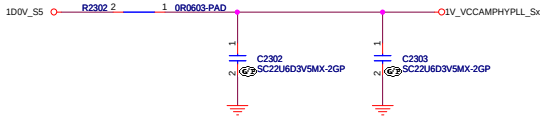
wistron

Wistron Incorporated
21F, 88, Sec.1,Hsin Tai Wu Rd
Hsichih, Taipei Hsien

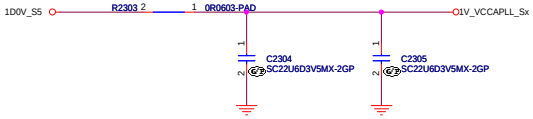
Title: PCH_(POWER2)

Size: C | Document Number: vHulk | Rev: -1

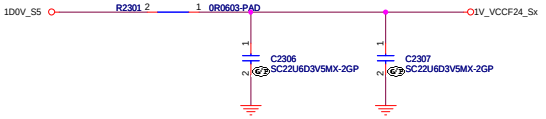
Date: Wednesday, September 23, 2015 | Sheet 22 of 107



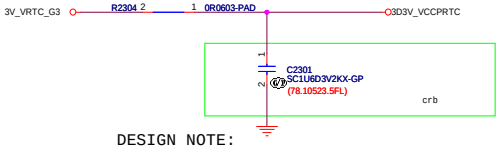
DESIGN NOTE:
PLACE HOLDER FOR VCCMPHYPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN A42,A43, AND B43



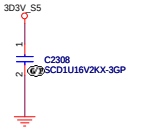
DESIGN NOTE:
PLACE HOLDER FOR VCCAUSB_1P0 AND VCCAAZPLL_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN AJ5,AL5, AND AN19



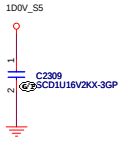
DESIGN NOTE:
PLACE HOLDER FOR VCCF24_1P0 FILTER
CAD NOTE:
PLACE CLOSE TO PCH PIN
PIN K2 AND K3



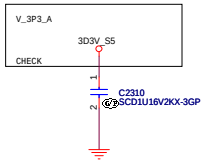
DESIGN NOTE:
BOARD CAP FOR VCCPRTC_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA22



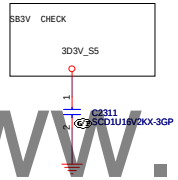
DESIGN NOTE:
EDGE CAP FOR VCCPGPPEF(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AJ41 AND AL41



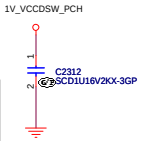
DESIGN NOTE:
BOAED CAP FOR VCCMPHY_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26



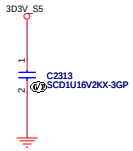
DESIGN NOTE:
EDGE CAP FOR VCCPUSBDSW_3P3
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN W15



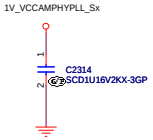
DESIGN NOTE:
BOAED CAP FOR VCCPRTCPRIM_3P3
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA20



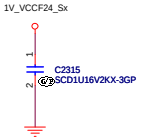
DESIGN NOTE:
BOAED CAP FOR VCCDSW_1P0
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN BA29



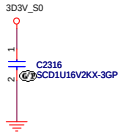
DESIGN NOTE:
EDGE CAP FOR VCCPGPPG(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AD41



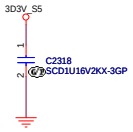
DESIGN NOTE:
BOAED CAP FOR VCCMPHYPLL_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN A42,A43 AND B43



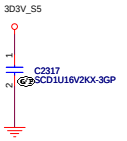
DESIGN NOTE:
BOAED CAP FOR VCCF24_1P0(PLACE HOLDER)
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN K2,K3



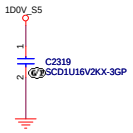
DESIGN NOTE:
BOAED CAP FOR VCCATS
CAD NOTE:
PLACE 3~5MM FROM PACKAGE EDGE
PIN AD13



DESIGN NOTE:
EDGE CAP FOR VCCPGPPBCH(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN BC42 AND BD40



DESIGN NOTE:
BOAED CAP FOR VCCPHVC_3P3(PLACE HOLDER)
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN AN15



DESIGN NOTE:
EDGE CAP FOR VCCMPHY_1P0 AND VCCDUSB_1P0
CAD NOTE:
PLACE 1~3MM FROM PACKAGE EDGE
PIN U21,U23,U25,U26,V26,AND AC17

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Hsichih, Taipei Hsien

Title: PCH Power CAP

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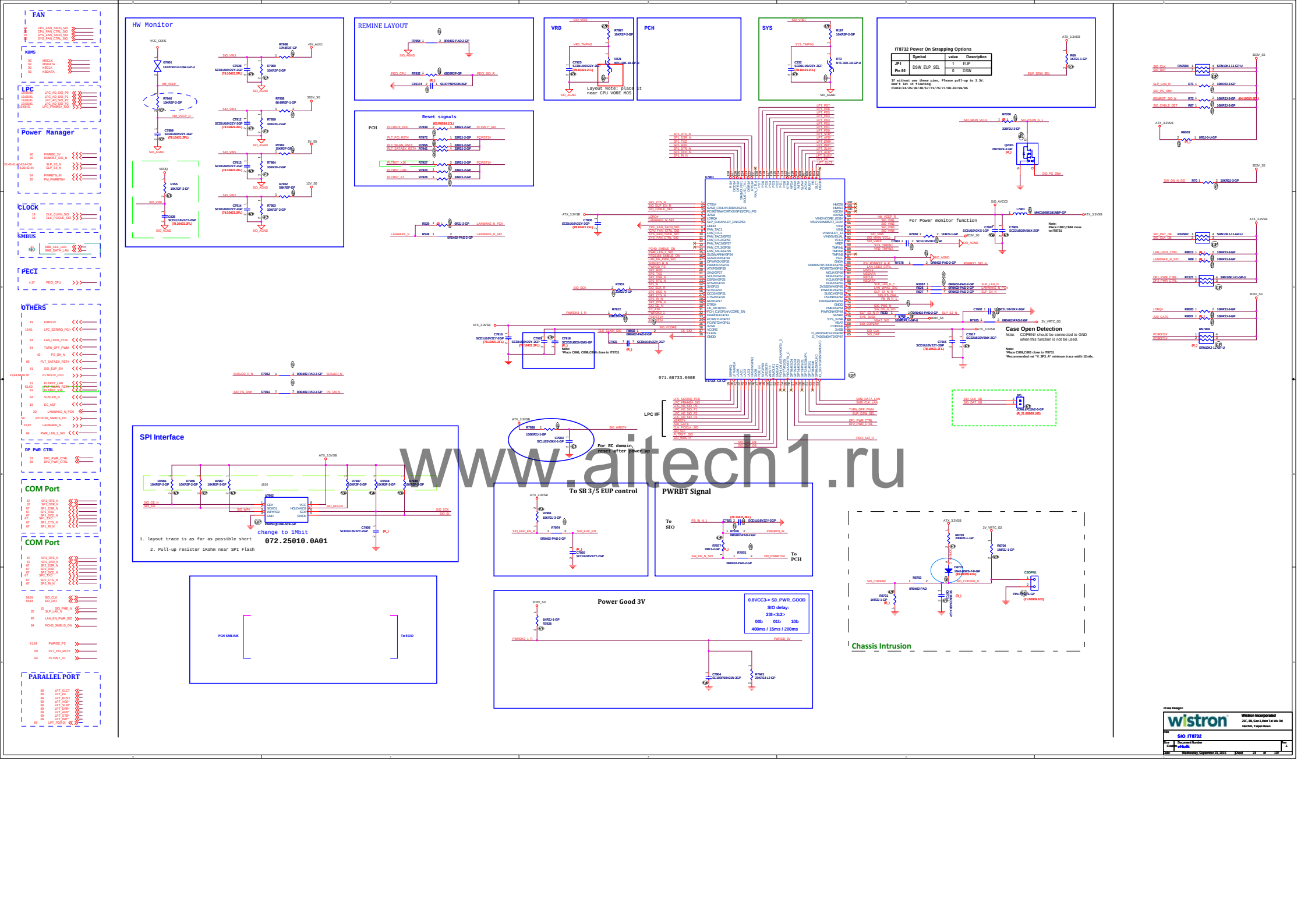

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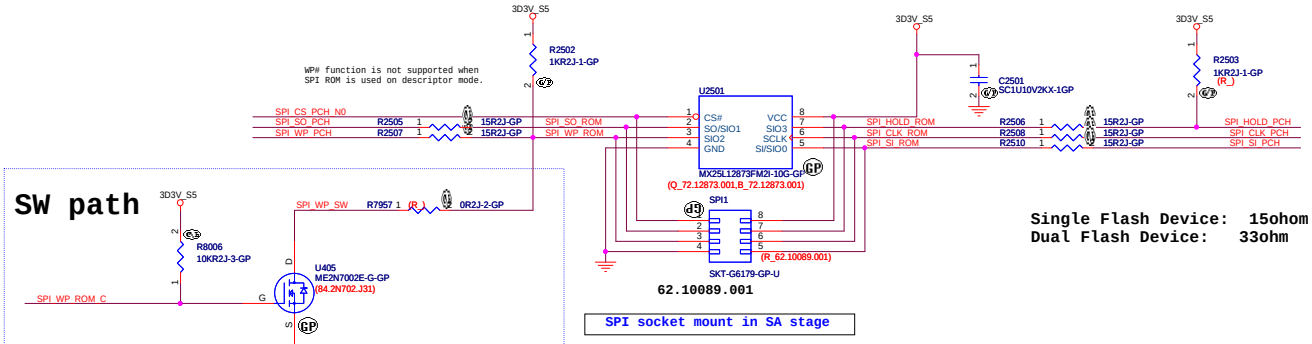
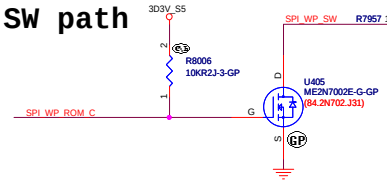
15 SPI_CS_PCH_N0
15,22 SPI_SO_PCH
15,22,99 SPI_WP_PCH
15,22 SPI_HOLD_PCH
15 SPI_CLK_PCH
15,22 SPI_SI_PCH
15 SPI_WP_ROM_C
15 SPI_WP_ROM_C2

SPI ROM

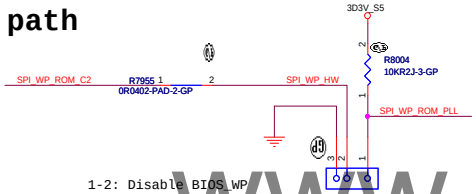


SW path



Single Flash Device: 15ohm
Dual Flash Device: 33ohm

SPI Write Protect HW path



SPI ROM TABLE

	Vendor	Package	SA	SB
Q170/B150	MXIC	SOP8 / 16MB	72.12873.001	72.12873.001
	WINBOND	SOP8 / 16MB	72.25128.0E1	72.25128.0E1

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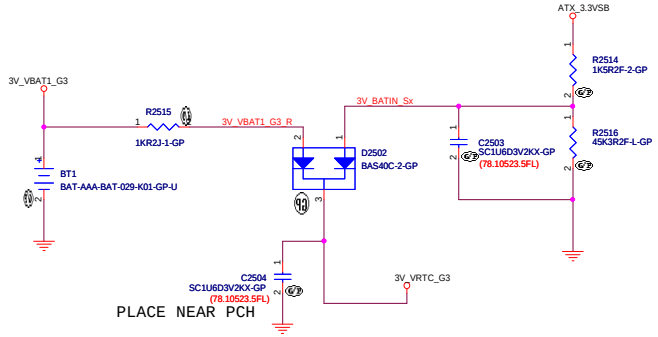
VCCRTC



SKL Platforms – SPI0_IO3 Signal Implementation Requirement for ES or pre-ES1/ES1 Samples

An Intel internal debug strap is implemented on the SPI0_IO3 signal. However, the strap is not functioning as expected on ES (SKL U/Y platform) and pre-ES1/ES1 (SKL S/H platform) samples and could prevent the system from booting. The issue will be fixed in future samples.

To ensure the platform boots with these early samples, Intel recommends customers to implement a pull-down resistor on the SPI0_IO3 signal aside from the 1 kOhm pull-up resistor which is already a requirement on the signal. There are two options to implement the pull-down resistor:

Option 1: Implement a 1 kOhm pull-down resistor on the signal and de-populate the required 1 kOhm pull-up resistor. In this case, customers must ensure that the SPI flash device on the platform has HOLD functionality disabled by default.

Option 2: Implement a strong pull-down resistor (e.g. 100 Ohm) on the signal and disable it after RSMRST# de-assertion.

Note that the pull down resistor on SPI0_IO3 is only needed for SKL U/Y platforms with ES and SKL S/H platforms with pre-ES1/ES1 samples.

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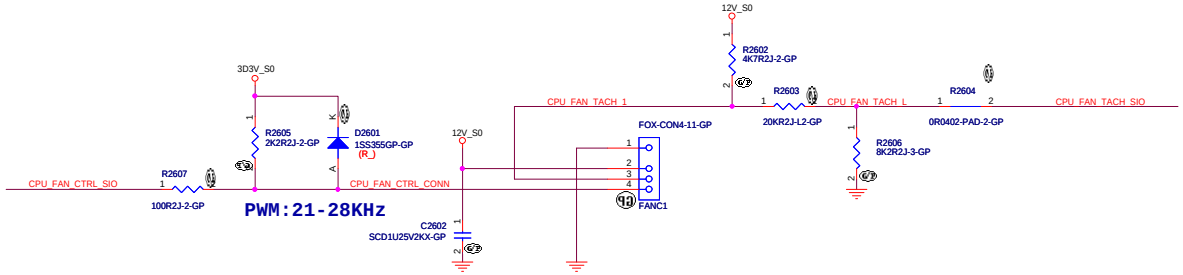
24 CPU_FAN_CTRL_SIO
24 CPU_FAN_TACH_SIO
24 SYS_FAN_CTRL_SIO
24 SYS_FAN_TACH_SIO

CPU FAN



SYS FAN

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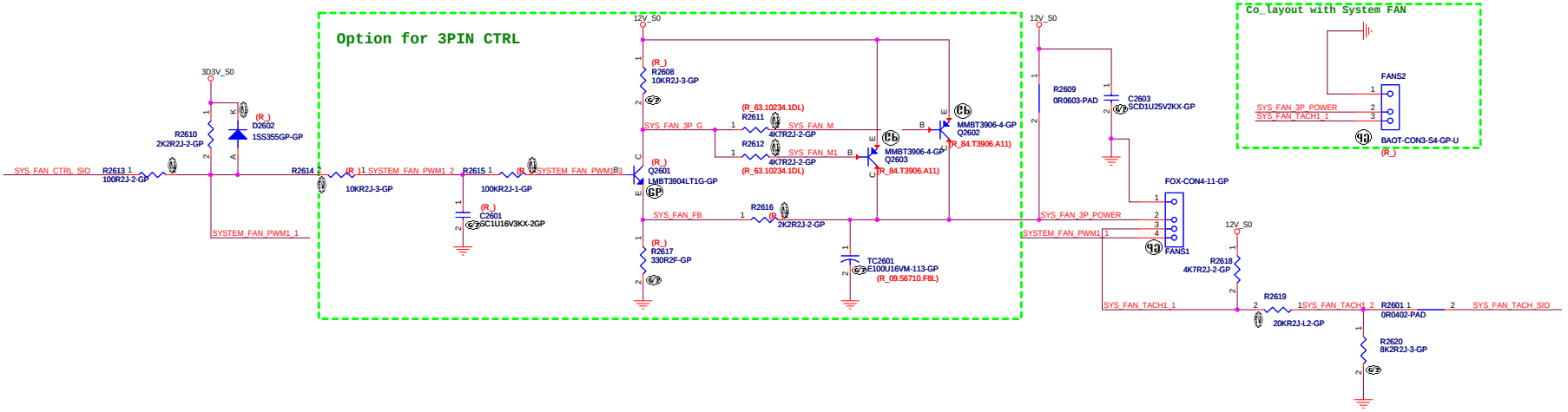
SYS 3 PINS/4 PINS FAN CONTROL



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Title: Thermal & FAN

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	ALC662-VC\VD
Line-in	pin23/24
Line-out	pin35/36
Mic-in 1	pin21/22
Mic-in 2	pin16/17
FP-out	pin14/15

HD_LINK

20	HDA_SDIN0_PCH
20	HDA_SDOUT_CODEC
20,27	HDA_RST#_CODEC
20	HDA_SYNC_CODEC
20	HDA_BITCLK_CODEC

AUDIO REAR PORT

30	AUD_IN_L
30	AUD_IN_R
30	AUDAMPIN_L
30	AUDAMPIN_R
30	MIC1_VREFO_L
30	AUD_MIC1_L
30	AUD_MIC1_R
30	MIC1_VREFO_R
30	SENSE_A

AUDIO FRONT HEADER

29	SENSE_B
29	MIC2-VREFO
29	FP_MIC2_L
29	FP_MIC2_R
29	FP_OUT_L
29	FP_OUT_R
29	LINE2_VREFO

MISC

20,27	HDA_RST#_CODEC
29,30	MUTE

Close to Pin 25

Close to Pin 38

11/21 Add C2930 C2931

Analog Digital

Close to Pin 38

Close to codec

ALC662-VD-GR-GP

71.00662.A0G

POP Circuit *Rear*

Control by software driver and CODEC GPIO.
GPIO driving low at:
1).Initial state
2).Suspend to S1
3).Resume from S1.

Layout: separately placed around AGND and GND

Audio Internal Speaker Header

Layout close to C5811

Add & reserve 0.1uF for pop-noise
05/05

DIGITAL ANALOG

Control circuit

Control line

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Title: Audio Codec_ALC662

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Title: AMP_(R)

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15 FP_AUDIO_PRESENCE_N

27 SENSE_B

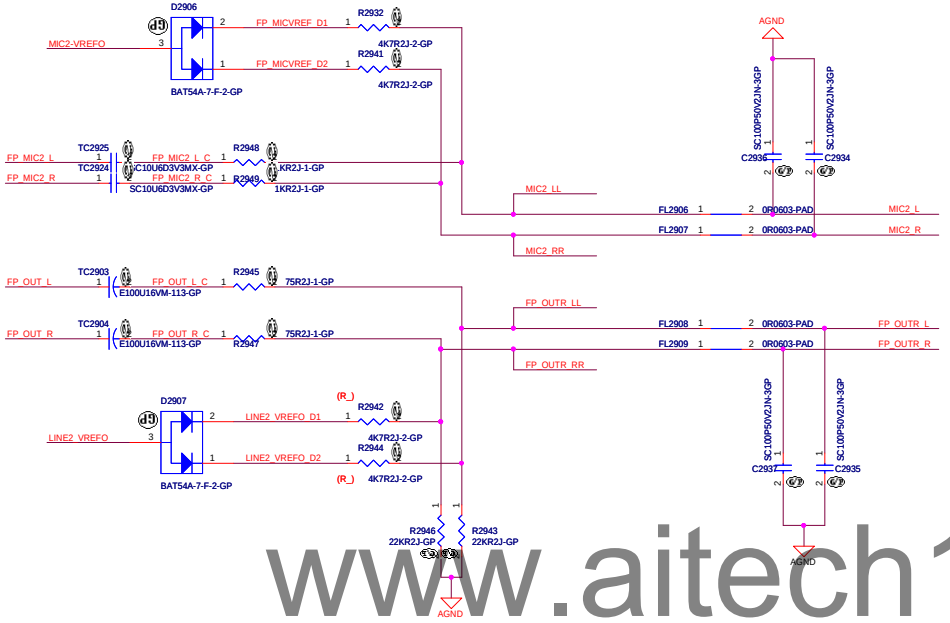
27 MIC2-VREFO

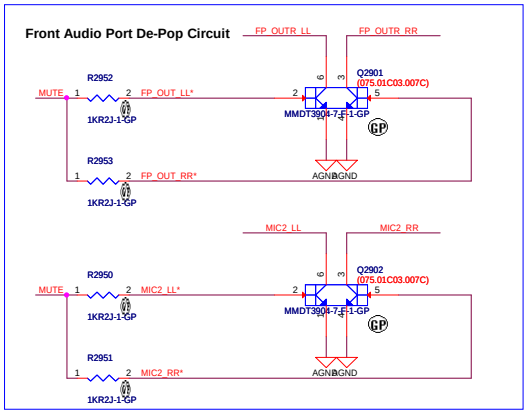
27 FP_MIC2_L
27 FP_MIC2_R

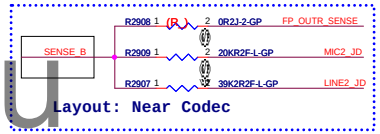
27 FP_OUT_L
27 FP_OUT_R

27 LINE2_VREFO

27,30 MUTE







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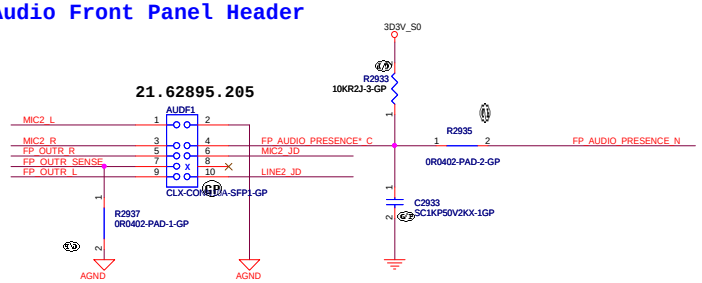
Audio Front Panel Header



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Title: Audio IO_Front

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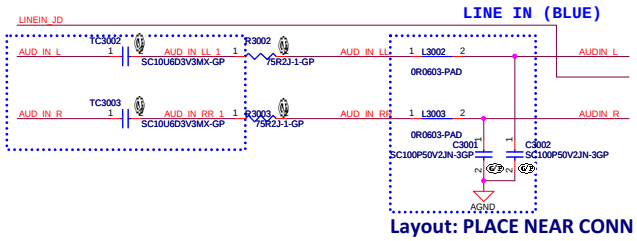
BACK PANEL PHONJACKS

AUDIO REAR PORT

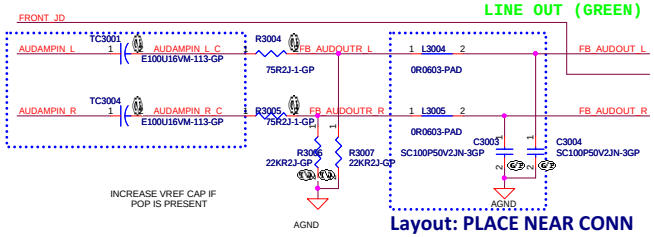
27 AUD_IN_L
27 AUD_IN_R
27 AUDAMPIN_L
27 AUDAMPIN_R
27 MIC1_VREFO_L
27 AUD_MIC1_L
27 AUD_MIC1_R
27 MIC1_VREFO_R
27 SENSE_A
27,29 MUTE

The cap need to close codec on layout.

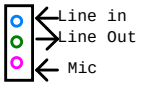


Layout: PLACE NEAR CONN

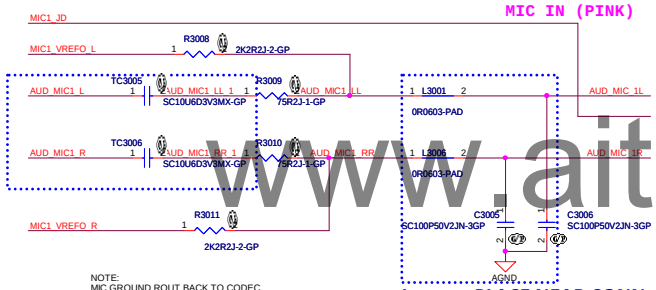
The cap need to close codec on layout.



Layout: PLACE NEAR CONN

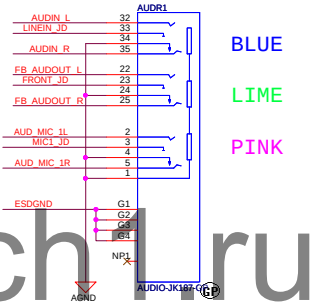


The cap need to close codec on layout.



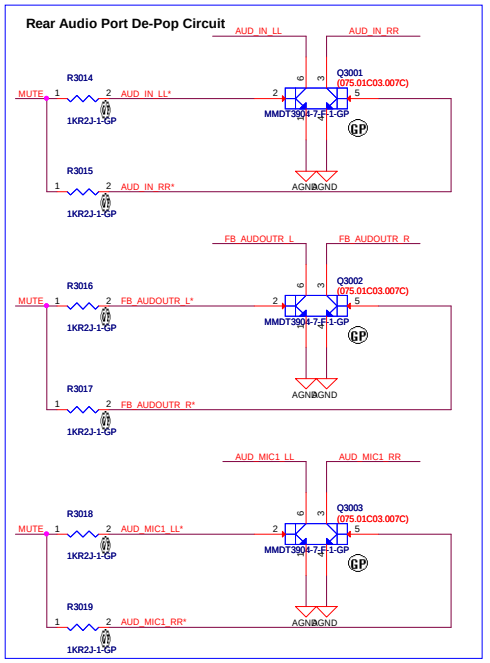
NOTE:
MIC GROUND ROUT BACK TO CODEC
ALONG WITH MIC_TRACE.
TIE MIC_GND TO AGND NEAR CODEC

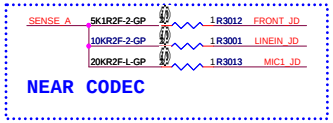
Layout: PLACE NEAR CONN



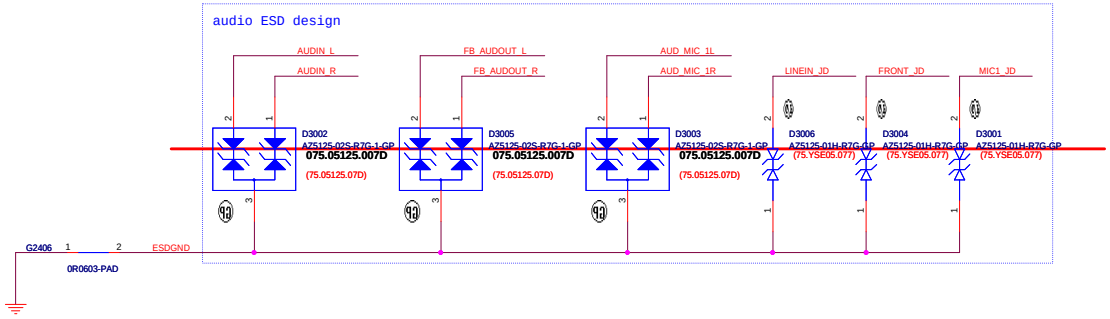
BLUE
LIME
PINK

22.10251.831





NEAR CODEC



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MDI

32,97	LAN_MDI_LAN_P0
32,97	LAN_MDI_LAN_N0
32,97	LAN_MDI_LAN_P1
32,97	LAN_MDI_LAN_N1
32,97	LAN_MDI_LAN_P2
32,97	LAN_MDI_LAN_N2
32,97	LAN_MDI_LAN_P3
32,97	LAN_MDI_LAN_N3

PCIE

18,97	PEG_CLK2_LAN
18,97	PEG_CLK2_LAN#
16,97	PCIE_TX_LAN_P5
16,97	PCIE_TX_LAN_N5
16,97	PCIE_RX_LAN_P5
16,97	PCIE_RX_LAN_N5

OTHERS

24	PLTRST_LAN
24,97	LANWAKE_N
18,97	PEG_CLKREQ2_LAN#

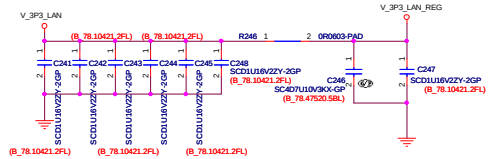
LAN LED

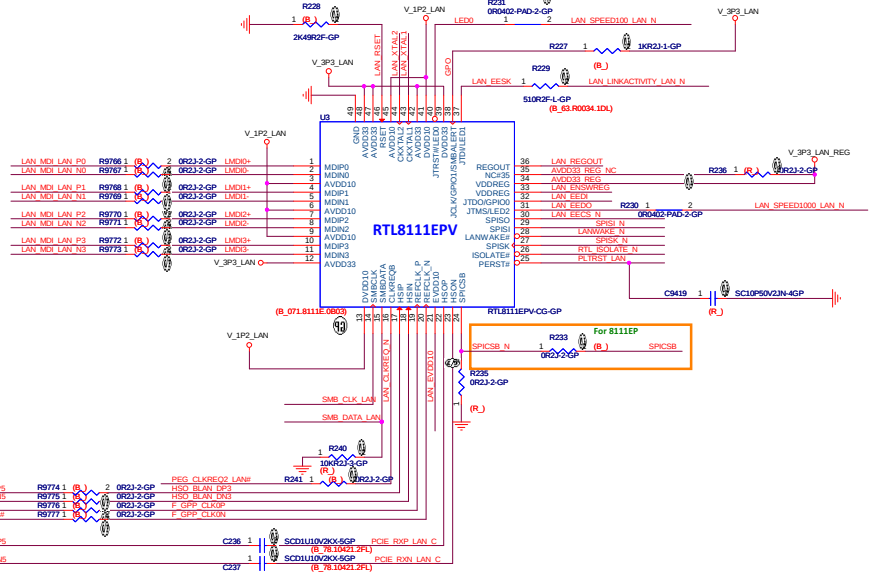
32,97	LAN_SPEED1000_LAN_N
32,97	LAN_SPEED100_LAN_N
32,64,97	LAN_LINKACTIVITY_LAN_N

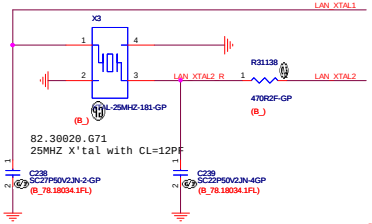
SMBUS

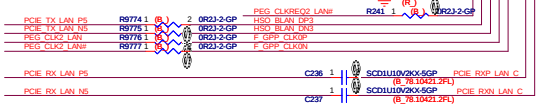
20	SML1CLK_PCH_DASH
20	SML1DATA_PCH_DASH
24	SMB_CLK_LAN
24	SMB_DATA_LAN

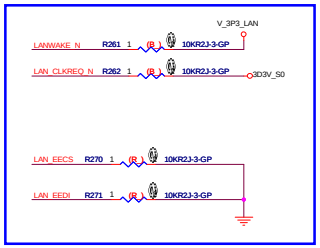
10Mb: Green
100Mb: Green
1Gb: Orange
Active: Green Light flash

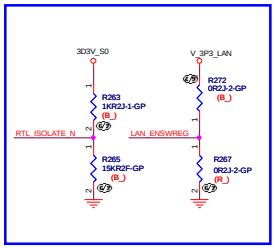


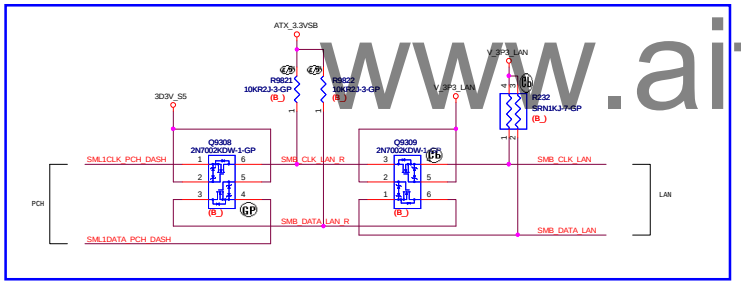


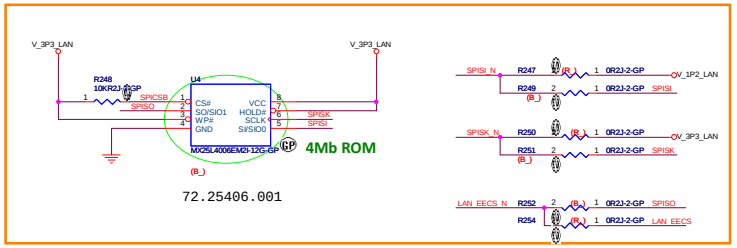


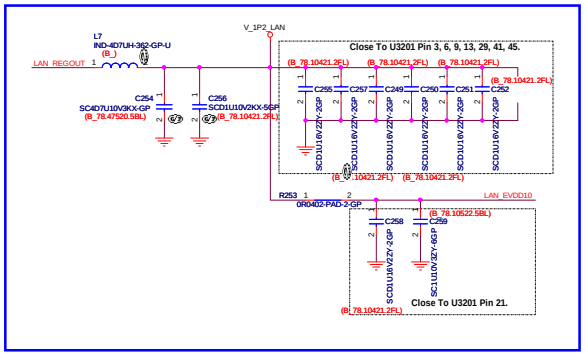












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Title: LAN_RTL8111EPV

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LAN

31,97 LAN_MDI_LAN_P0
31,97 LAN_MDI_LAN_N0
31,97 LAN_MDI_LAN_P1
31,97 LAN_MDI_LAN_N1
31,97 LAN_MDI_LAN_P2
31,97 LAN_MDI_LAN_N2
31,97 LAN_MDI_LAN_P3
31,97 LAN_MDI_LAN_N3
31,97 LAN_SPEED1000_LAN_N
31,97 LAN_SPEED100_LAN_N
31,64,97 LAN_LINKACTIVITY_LAN_N

LAN

36 USB_CON_PN10
36 USB_CON_PP10
36 USB_CON_PN11
36 USB_CON_PP11

EL3202
LAN_MDI_LAN_N3 2 1 LAN_MDI_CON_N3
LAN_MDI_LAN_P3 3 4 LAN_MDI_CON_P3
MCM1012B900FBP-GP-U
(66.R0036.04L)

EL3203
LAN_MDI_LAN_N1 2 1 LAN_MDI_CON_N1
LAN_MDI_LAN_P1 3 4 LAN_MDI_CON_P1
MCM1012B900FBP-GP-U
(66.R0036.04L)

EL3201
LAN_MDI_LAN_N2 2 1 LAN_MDI_CON_N2
LAN_MDI_LAN_P2 3 4 LAN_MDI_CON_P2
MCM1012B900FBP-GP-U
(66.R0036.04L)

EL3204
LAN_MDI_LAN_N0 2 1 LAN_MDI_CON_N0
LAN_MDI_LAN_P0 3 4 LAN_MDI_CON_P0
MCM1012B900FBP-GP-U
(66.R0036.04L)

	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

USB+RJ45

V_3P3_LAN
R2801 330R2J-3-GP (R_)
R2810 330R2J-3-GP (R_)
C2809 SCD1U16V2ZY-2GP (R_)
C2810 SCD1U16V2ZY-2GP (R_)
C2811 SCD1U16V2ZY-2GP (R_)
5V_USB20_RJUSB1
5V_USB20_RJUSB2
TC9408 E560U6D3VM-7-GP
U2RJ1
G2 G4 L4 LAN_LED_ACT
G6
L3 LAN_LINKACTIVITY_CON_N
R3207 510R2J-1-GP LAN_LINKACTIVITY_LAN_N
R10
R9 LAN_MDI_CON_N3
R8 LAN_MDI_CON_P3
R7 LAN_MDI_CON_N2
R6 LAN_MDI_CON_P2
R5 LAN_MDI_CON_N1
R4 LAN_MDI_CON_P1
R3 LAN_MDI_CON_N0
R2 LAN_MDI_CON_P0
R1 LAN_CONN_CVT
L2 LAN_SPEED100_CON_N
R3208 330R3J-L-GP LAN_SPEED100_LAN_N
L1 LAN_SPEED1000_CON_N
R3209 330R3J-L-GP LAN_SPEED1000_LAN_N
G3 G1
G5 G7
U5 U1 U6 U2 U7 U3 U8 U4
USB_CON_PN10 USB_CON_PN11 USB_CON_PP10 USB_CON_PP11
C2813 SCD1U16V2ZY-2GP (R_)
C2812 SCD1U16V2ZY-2GP (R_)
RJ45-USB-LED-8-GP
(W_022.10001.0F51_S_022.10001.0A81)
022.10001.0F51

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ESD

V_3P3_LAN
ED3201
LAN_MDI_CON_N0 1 I/O1 I/O4 6 LAN_MDI_CON_P0
2 GND VDD 5
LAN_MDI_CON_P1 3 I/O2 I/O3 4 LAN_MDI_CON_N1
AZC099-04S-R7G-GP
(075.00005.0B7C)
C3204 SCD1U16V2KX-3GP

V_3P3_LAN
ED3203
LAN_MDI_CON_N2 1 I/O1 I/O4 6 LAN_MDI_CON_P2
2 GND VDD 5
LAN_MDI_CON_P3 3 I/O2 I/O3 4 LAN_MDI_CON_N3
AZC099-04S-R7G-GP
(075.00005.0B7C)
C3207 SCD1U16V2KX-3GP

LAN_LINKACTIVITY_CON_N
C3208 SC470P50V2KX-3GP (R_)
LAN_SPEED1000_CON_N
C3206 SC470P50V2KX-3GP (R_)
LAN_SPEED100_CON_N
C3201 SC470P50V2KX-3GP (R_)
For EMC

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Title: RJ45&Transformer
Size: C
Document Number: vHulk
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Title: Card Reader_(R)

Size	Document Number	Rev
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Title: USB Charger_(R)

Size	Document Number	Rev
C	vHulk	-1

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Title: USB_Redrive_(R)

Size	Document Number	Rev
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USB 2.0 Rear Signals for RJ45/USB2.0 Stack

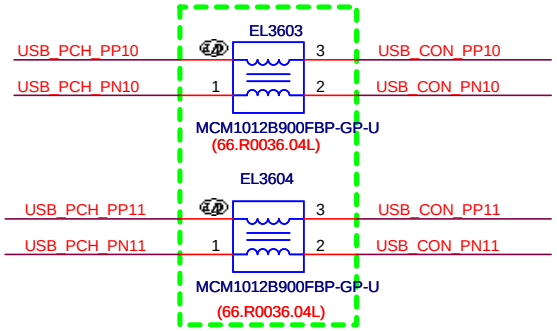
USB 2.0 Rear Signals for RJ45/USB2.0 Stack

16 USB_PCH_PP10
16 USB_PCH_PN10

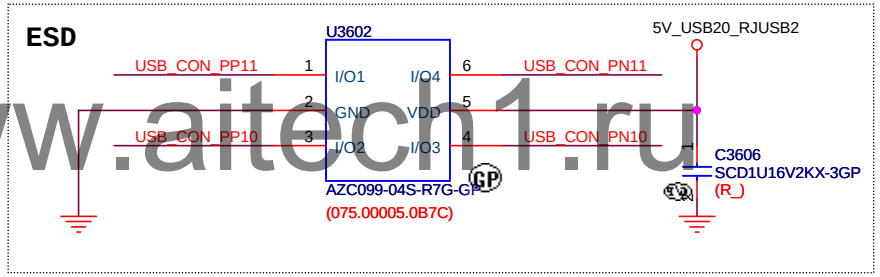
16 USB_PCH_PP11
16 USB_PCH_PN11

32 USB_CON_PP10
32 USB_CON_PN10

32 USB_CON_PP11
32 USB_CON_PN11



DESIGN NOTE:
To U2RJ1(U2+RJ45 CONN)
IF SI Concern, Change CMC PN:068.01012.2001



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Title: USB 20_REAR PORT

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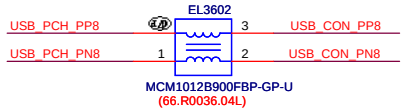
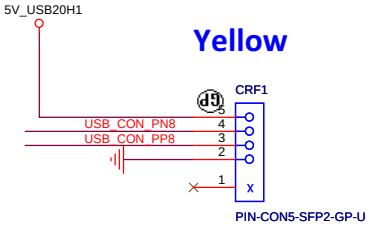
16 USB_PCH_PP8
16 USB_PCH_PN8

16 USB_PCH_PP9
16 USB_PCH_PN9

16 USB_PCH_PP7
16 USB_PCH_PN7

CR HEADER





Yellow

21.62967.105

ESD

USB2.0 FRONT HEADER

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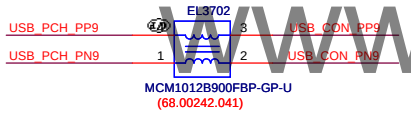

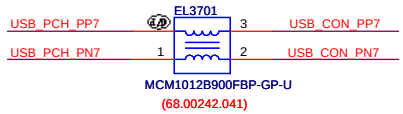

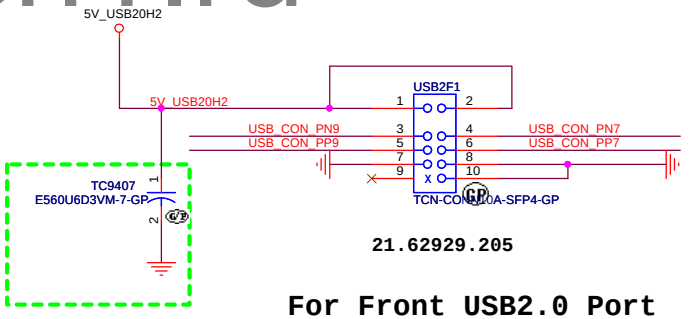

21.62929.205

For Front USB2.0 Port

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Title: USB20_FRONT HEADER

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USB3.0 REAR CONNECTOR

19 USB30_RX_PCH_N5
19 USB30_RX_PCH_P5
19 USB30_TX_PCH_N5
19 USB30_TX_PCH_P5

19 USB30_RX_PCH_N4
19 USB30_RX_PCH_P4
19 USB30_TX_PCH_N4
19 USB30_TX_PCH_P4

16 USB_PCH_PP1
16 USB_PCH_PN1

16 USB_PCH_PP4
16 USB_PCH_PN4

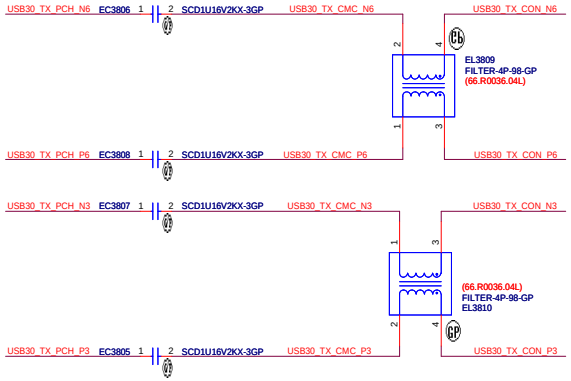
16 USB_PCH_PN2
16 USB_PCH_PP2

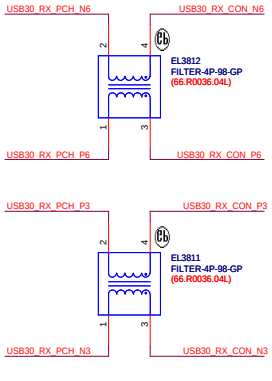
16 USB_PCH_PP3
16 USB_PCH_PN3

19 USB30_TX_PCH_N6
19 USB30_TX_PCH_P6
19 USB30_RX_PCH_N6
19 USB30_RX_PCH_P6

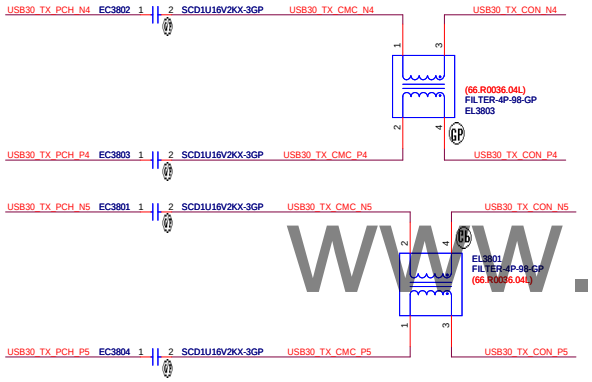
19 USB30_TX_PCH_N3
19 USB30_TX_PCH_P3
19 USB30_RX_PCH_N3
19 USB30_RX_PCH_P3

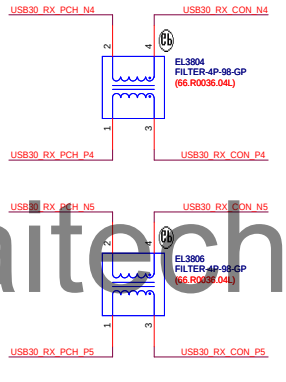
USB3.0 EMI





USB3.0 EMI





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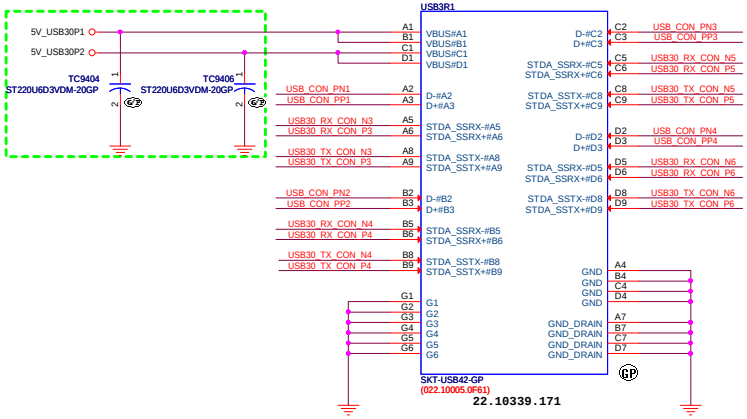
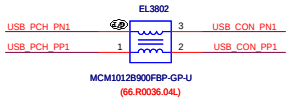
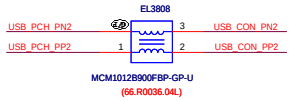
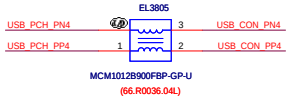
USB3.0 REAR PORT1

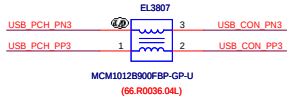


EMI



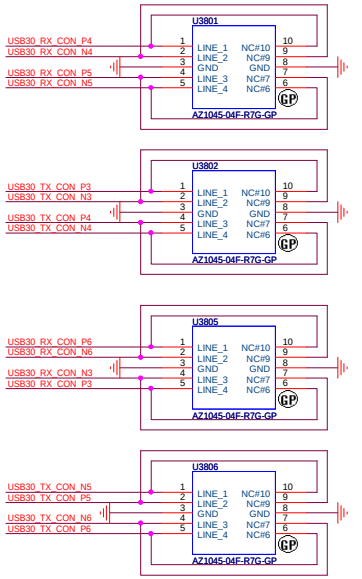


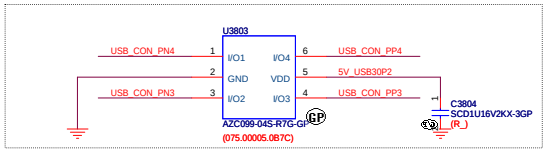


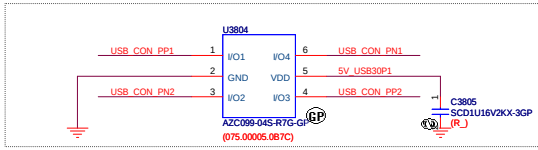


EMI

ESD







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Title: USB30_REAR PORT

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USB3.0 FRONT HEADER

19 USB30_RX_PCH_N1
19 USB30_RX_PCH_P1
19 USB30_TX_PCH_N1
19 USB30_TX_PCH_P1

19 USB30_RX_PCH_N2
19 USB30_RX_PCH_P2
19 USB30_TX_PCH_N2
19 USB30_TX_PCH_P2

16 USB_PCH_PN5
16 USB_PCH_PP5

16 USB_PCH_PP6
16 USB_PCH_PN6

16 USB30_RX_PCH_N7
16 USB30_RX_PCH_P7
16 USB30_TX_PCH_N7
16 USB30_TX_PCH_P7

16 USB30_TX_PCH_N8
16 USB30_TX_PCH_P8
16 USB30_RX_PCH_N8
16 USB30_RX_PCH_P8

16 USB_PCH_PP13
16 USB_PCH_PN13

16 USB_PCH_PP14
16 USB_PCH_PN14

USB3.0 EMI

USB30_TX_PCH_N1 EC3902 1 2 SCD1U16V2KX-3GP USB30_TX_CMC_N1 USB30_TX_CON_N1

(66.R0036.04L) FILTER-4P-98-GP EL3902

USB30_TX_PCH_P1 EC3903 1 2 SCD1U16V2KX-3GP USB30_TX_CMC_P1 USB30_TX_CON_P1

USB30_TX_PCH_N2 EC3901 1 2 SCD1U16V2KX-3GP USB30_TX_CMC_N2 USB30_TX_CON_N2

(66.R0036.04L) FILTER-4P-98-GP EL3901

USB30_TX_PCH_P2 EC3904 1 2 SCD1U16V2KX-3GP USB30_TX_CMC_P2 USB30_TX_CON_P2

USB30_RX_PCH_N1 USB30_RX_CON_N1

(66.R0036.04L) FILTER-4P-98-GP EL3903

USB30_RX_PCH_P1 USB30_RX_CON_P1

USB30_RX_PCH_N2 USB30_RX_CON_N2

(66.R0036.04L) FILTER-4P-98-GP EL3906

USB30_RX_PCH_P2 USB30_RX_CON_P2

EMI

EL3904

USB_PCH_PN5 USB_CON_PN5
USB_PCH_PP5 USB_CON_PP5

CMC:
INPAQ: 068.01012.2011
PANASONIC: 068.24900.2001
MURATA: 68.00396.001

MCM1012B900FBP-GP-U (66.R0036.04L)

EL3905

USB_PCH_PN6 USB_CON_PN6
USB_PCH_PP6 USB_CON_PP6

CMC:
INPAQ: 068.01012.2011
PANASONIC: 068.24900.2001
MURATA: 68.00396.001

MCM1012B900FBP-GP-U (66.R0036.04L)

U3903

USB_CON_PN5 I/O1 I/O4 USB_CON_PP5
GND VDD 5V_USB30H1
USB_CON_PP6 I/O2 I/O3 USB_CON_PN6

AZC099-04S-R7G-GP (075.00005.0B7C)

C3903 SCD1U16V2KX-3GP

ESD

U3901 (R)

USB30_RX_CON_N1 LINE_1 NC#10
USB30_RX_CON_P1 LINE_2 NC#9
GND GND
USB30_RX_CON_N2 LINE_3 NC#7
USB30_RX_CON_P2 LINE_4 NC#6

AZ1045-04F-R7G-GP

U3902 (R)

USB30_TX_CON_N1 LINE_1 NC#10
USB30_TX_CON_P1 LINE_2 NC#9
GND GND
USB30_TX_CON_N2 LINE_3 NC#7
USB30_TX_CON_P2 LINE_4 NC#6

AZ1045-04F-R7G-GP

5V_USB30H1

C2735 SC22U6D3V5MX-2GP
C2737 SC22U6D3V5MX-2GP

USB3.0 FRONT HEADER 1

USB3F1

VBUS VBUS
INTA_P1_SSRX+ INTA_P1_SSRX-
INTA_P2_SSRX+ INTA_P2_SSRX-
INTA_P1_SSTX+ INTA_P1_SSTX-
INTA_P2_SSTX+ INTA_P2_SSTX-
INTA_P1_D+ INTA_P1_D-
INTA_P2_D+ INTA_P2_D-
ID EMPTY_PIN
GND GND GND GND

USB30_RX_CON_P1 USB30_RX_CON_N1 USB30_RX_CON_P2 USB30_RX_CON_N2
USB30_TX_CON_P1 USB30_TX_CON_N1 USB30_TX_CON_P2 USB30_TX_CON_N2
USB_CON_PP5 USB_CON_PN5 USB_CON_PP6 USB_CON_PN6

LOTES-CONN20C-SFP1-GP

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USB3.0 EMI

USB30_TX_PCH_N7 EC3906 1 2 SCD1U16V2KX-3GP USB30_TX_CMC_N7 USB30_TX_CON_N7

(Q_66.R0036.04L) FILTER-4P-98-GP EL3909

USB30_TX_PCH_P7 EC3908 1 2 SCD1U16V2KX-3GP USB30_TX_CMC_P7 USB30_TX_CON_P7

USB30_TX_PCH_N8 EC3907 1 2 SCD1U16V2KX-3GP USB30_TX_CMC_N8 USB30_TX_CON_N8

(Q_66.R0036.04L) FILTER-4P-98-GP EL3910

USB30_TX_PCH_P8 EC3905 1 2 SCD1U16V2KX-3GP USB30_TX_CMC_P8 USB30_TX_CON_P8

USB30_RX_PCH_N7 USB30_RX_CON_N7

(Q_66.R0036.04L) FILTER-4P-98-GP EL3911

USB30_RX_PCH_P7 USB30_RX_CON_P7

USB30_RX_PCH_N8 USB30_RX_CON_N8

(Q_66.R0036.04L) FILTER-4P-98-GP EL3912

USB30_RX_PCH_P8 USB30_RX_CON_P8

EMI

EL3908

USB_PCH_PP13 USB_CON_PP13
USB_PCH_PN13 USB_CON_PN13

CMC:
INPAQ: 068.01012.2011
PANASONIC: 068.24900.2001
MURATA: 68.00396.001

MCM1012B900FBP-GP-U (Q_66.R0036.04L)

EL3907

USB_PCH_PP14 USB_CON_PP14
USB_PCH_PN14 USB_CON_PN14

CMC:
INPAQ: 068.01012.2011
PANASONIC: 068.24900.2001
MURATA: 68.00396.001

MCM1012B900FBP-GP-U (Q_66.R0036.04L)

ESD

U3904 (R)

USB30_RX_CON_N7 LINE_1 NC#10
USB30_RX_CON_P7 LINE_2 NC#9
GND GND
USB30_RX_CON_N8 LINE_3 NC#7
USB30_RX_CON_P8 LINE_4 NC#6

AZ1045-04F-R7G-GP

U3905 (R)

USB30_TX_CON_N7 LINE_1 NC#10
USB30_TX_CON_P7 LINE_2 NC#9
GND GND
USB30_TX_CON_N8 LINE_3 NC#7
USB30_TX_CON_P8 LINE_4 NC#6

AZ1045-04F-R7G-GP

U3906

USB_CON_PN13 I/O1 I/O4 USB_CON_PP13
GND VDD 5V_USB30H2
USB_CON_PP14 I/O2 I/O3 USB_CON_PN14

AZC099-04S-R7G-GP (Q_075.00005.0B7C)

C3905 SCD1U16V2KX-3GP (Q_)

5V_USB30H2

C2736 SC22U6D3V5MX-2GP (Q_)
C2738 SC22U6D3V5MX-2GP (Q_)

USB3.0 FRONT HEADER2(Q170 SKU)

USB3F2

VBUS VBUS
INTA_P1_SSRX+ INTA_P1_SSRX-
INTA_P2_SSRX+ INTA_P2_SSRX-
INTA_P1_SSTX+ INTA_P1_SSTX-
INTA_P2_SSTX+ INTA_P2_SSTX-
INTA_P1_D+ INTA_P1_D-
INTA_P2_D+ INTA_P2_D-
ID EMPTY_PIN
GND GND GND GND

USB30_RX_CON_P7 USB30_RX_CON_N7 USB30_RX_CON_P8 USB30_RX_CON_N8
USB30_TX_CON_P7 USB30_TX_CON_N7 USB30_TX_CON_P8 USB30_TX_CON_N8
USB_CON_PP13 USB_CON_PN13 USB_CON_PP14 USB_CON_PN14

LOTES-CONN20C-SFP1-GP (Q_)

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Title: USB30_FRONT HEADER

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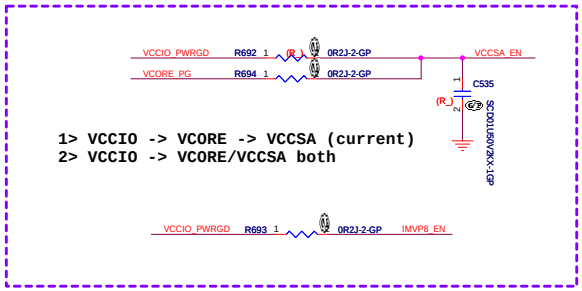
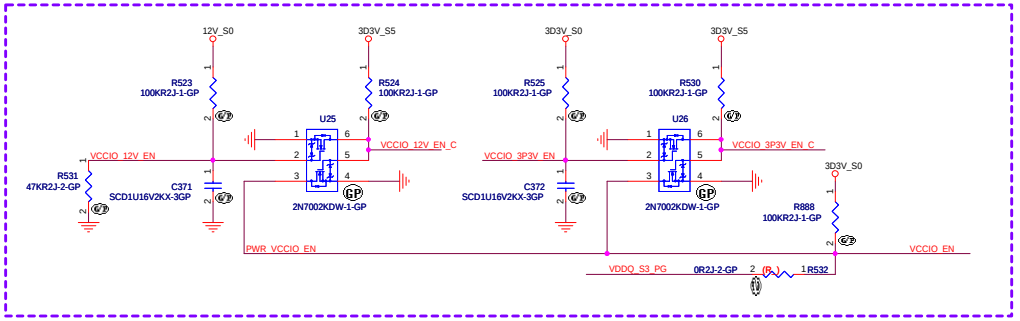
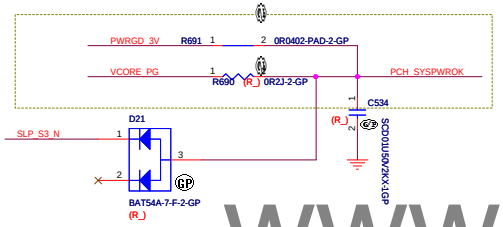
53 VCCIO_PWRGD
40,46 VCORE_PG
20,24,41,42,43,44,50 SLP_S3_N
20 PCH_SYSPWROK
52 VCCSA_EN
46 IMVP8_EN
24 PWRGD_3V
50 VDDQ_S3_PG
44,53 VCCIO_EN
40,46 VCORE_PG
52 VCCSA_PGOOD
4 CPU_VCCST_PWRGD
20 PCH_PWROK

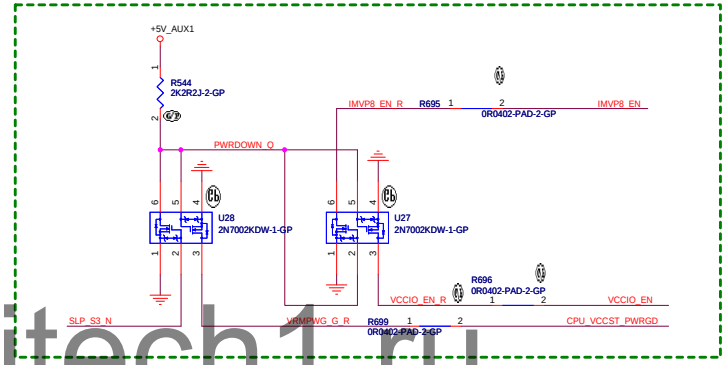
44,54 VPP_EN
44,50 VTT_EN
8,20,24,42,44 SLP_S4_N
44,50 VDDQ_EN
4,44 DDR_VTT_CNTL





Power Sequence





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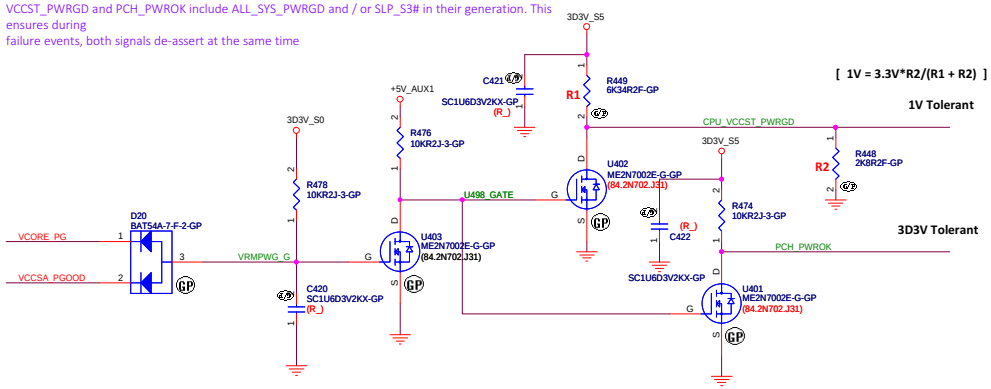
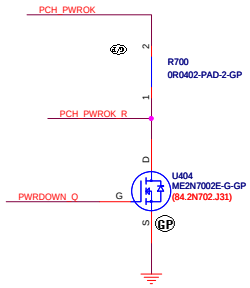
Note:
VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it. It is recommended that both
VCCST_PWRGD and PCH_PWROK include ALL_SYS_PWRGD and / or SLP_S3# in their generation. This ensures during
failure events, both signals de-assert at the same time





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Title: Power Plane EN Sequence

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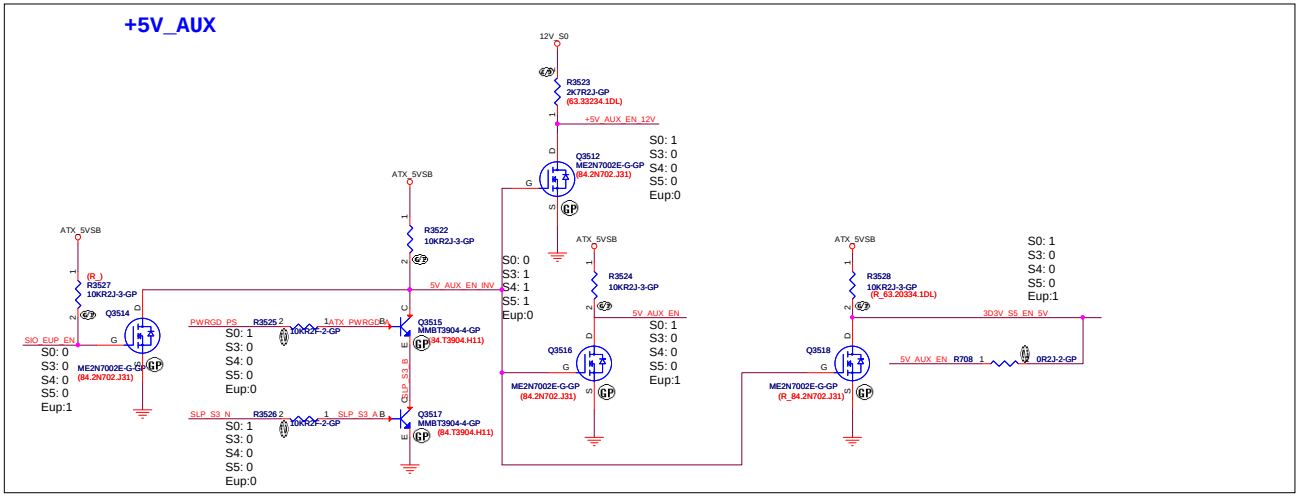
Dual Power Control

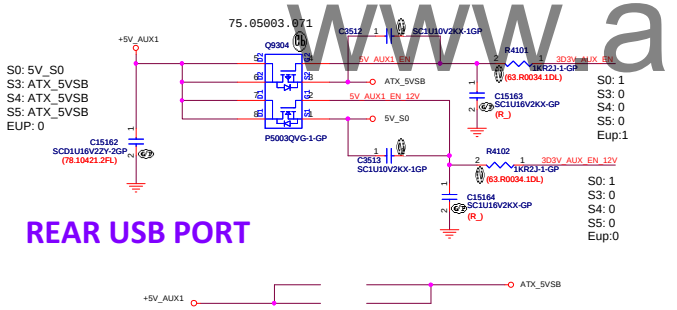
GROUP A POWER(S5_EuP)

24 SIO_EUP_EN
20,24,40,42,43,44,50 SLP_S3_N
24,49 PWRGD_PS

+5V_AUX

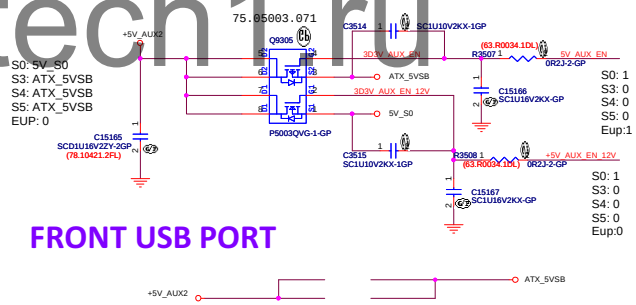


+5V_AUX1



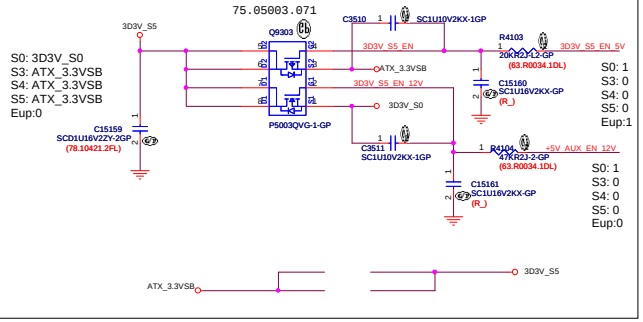
REAR USB PORT

+5V_AUX2



FRONT USB PORT

+3P3V_AUX



	SIO_EUP_EN	SLP_S3_N	+5V_AUX1	+5V_AUX2
S0	0	1	5V_S0	5V_S0
S3	0	0	ATX_5VSB	ATX_5VSB
S4	0	0	ATX_5VSB	ATX_5VSB
S5	0 (EUP Disable)	0	ATX_5VSB	ATX_5VSB
S5	1 (EUP Enable)	0	No Power	No Power

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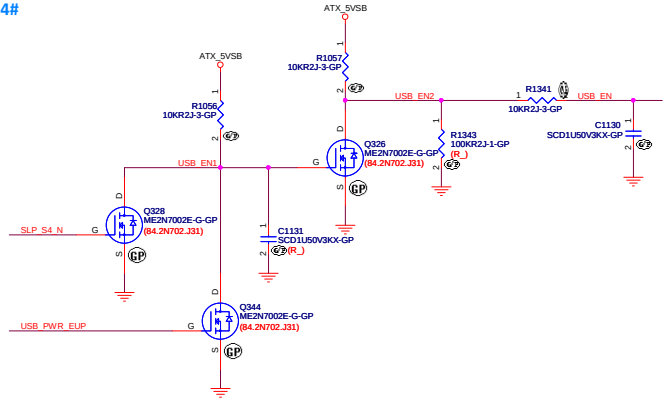
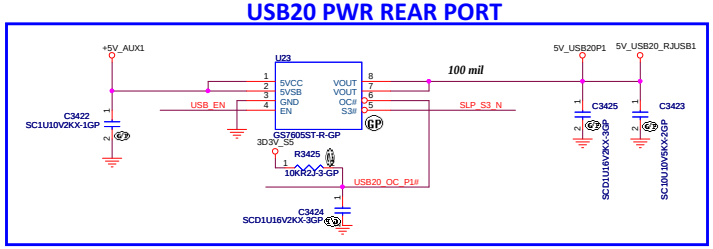
	S5	S4	S3-S0		S5	S4	S3-S0	Status
USB_PWR_SLP	L	L	L	USB_EN	L	L	H	No Support S4 USB wake up
USB_PWR_SLP	L	H	L	USB_EN	L	H	L	Support S4 USB wake up

S4, S5 --> choice by USB_PWR_SLP
S3-S0 --> choice by SLP_S4#

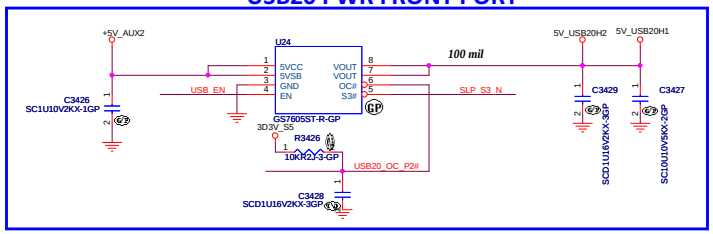
8,20,24,44 SLP_S4_N
20 USB_PWR_EUP
16 USB30_OC_P1#
16 USB30_OC_P2#
16 USB30_OC_H1#
16 USB30_OC_H2#
16 USB20_OC_P2#
16 USB20_OC_P1#
20,24,40,41,43,44,50 SLP_S3_N



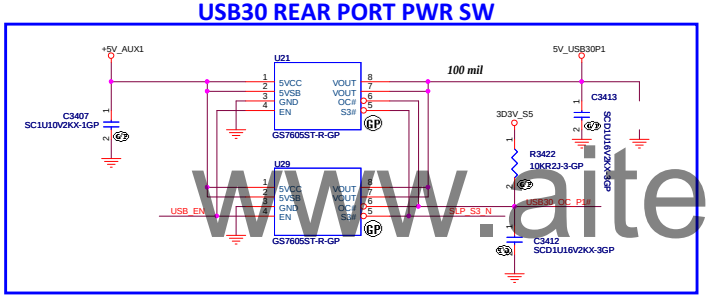
USB20 PWR REAR PORT



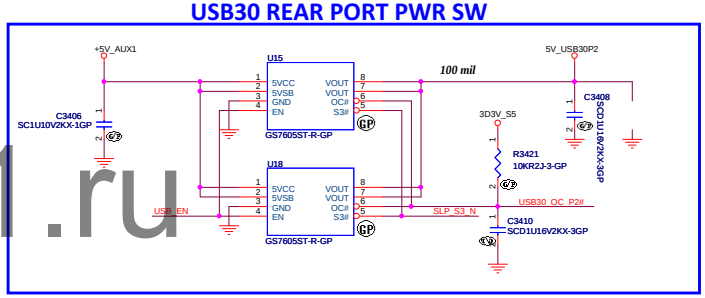
USB20 PWR FRONT PORT



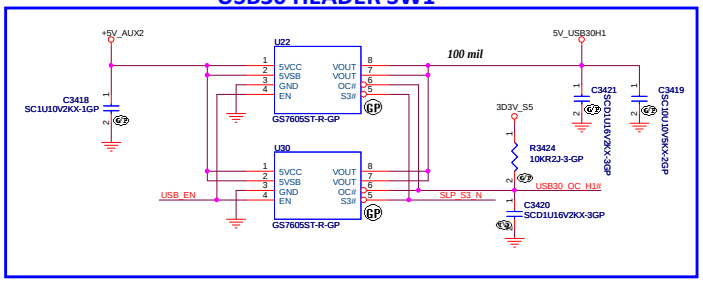
USB30 REAR PORT PWR SW



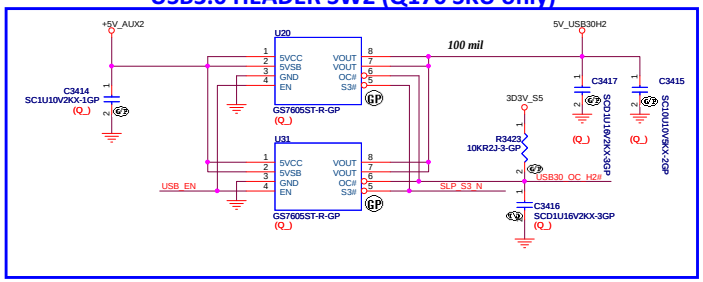
USB30 REAR PORT PWR SW



USB30 HEADER SW1



USB3.0 HEADER SW2 (Q170 SKU only)



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Title: Switch power
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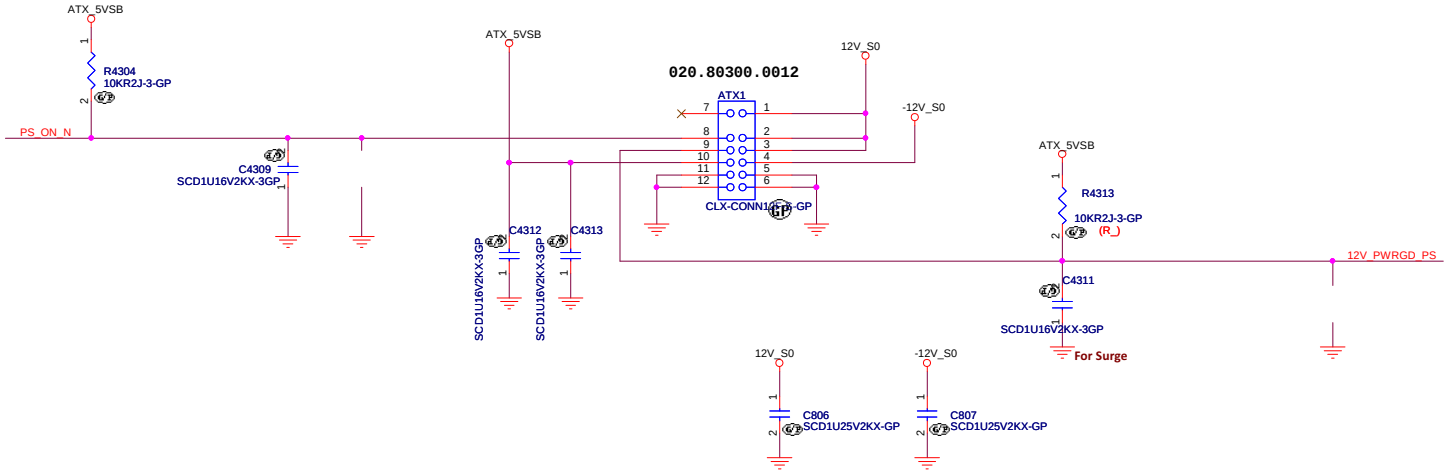
ATX CONNECTOR

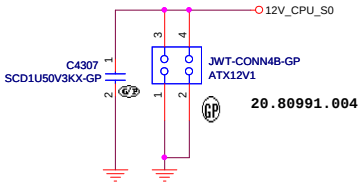


24 PS_ON_N

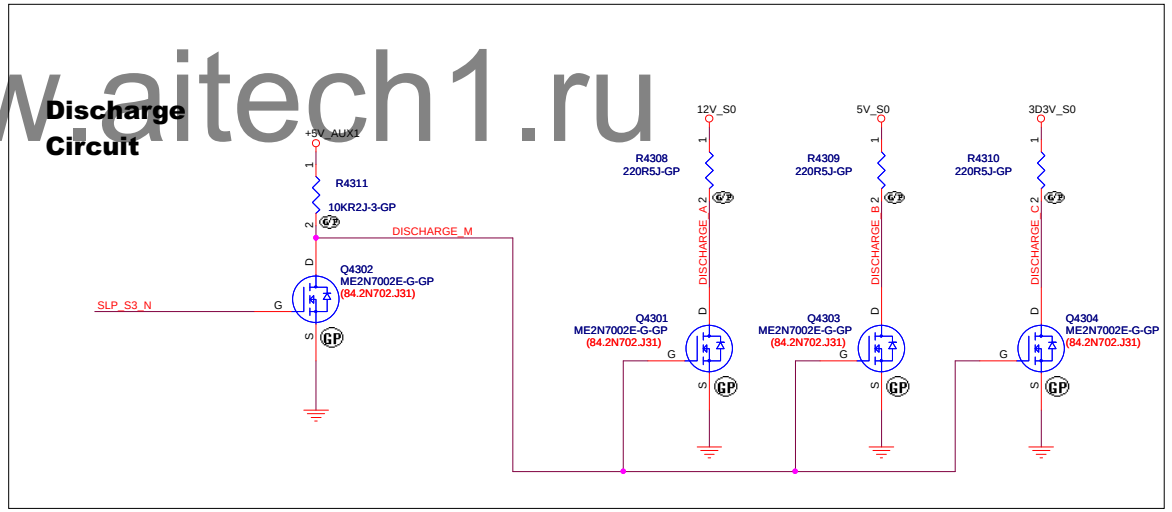
20,24,40,41,42,44,50 SLP_S3_N

49 12V_PWRGD_PS

CPU PWR CONN



Discharge Circuit



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Title: ATX

Size: Custom | Document Number: vHulk | Rev: -1

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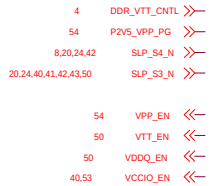

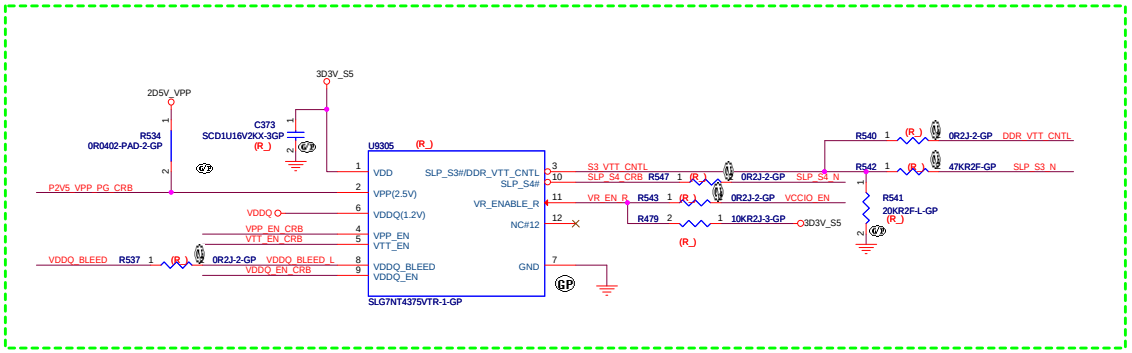

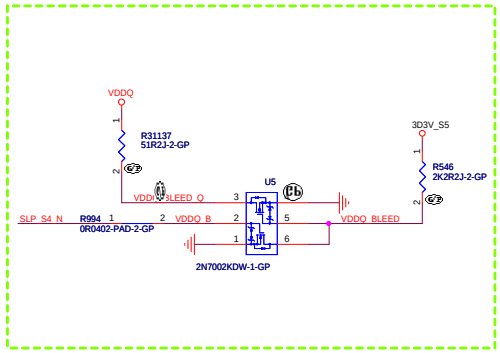

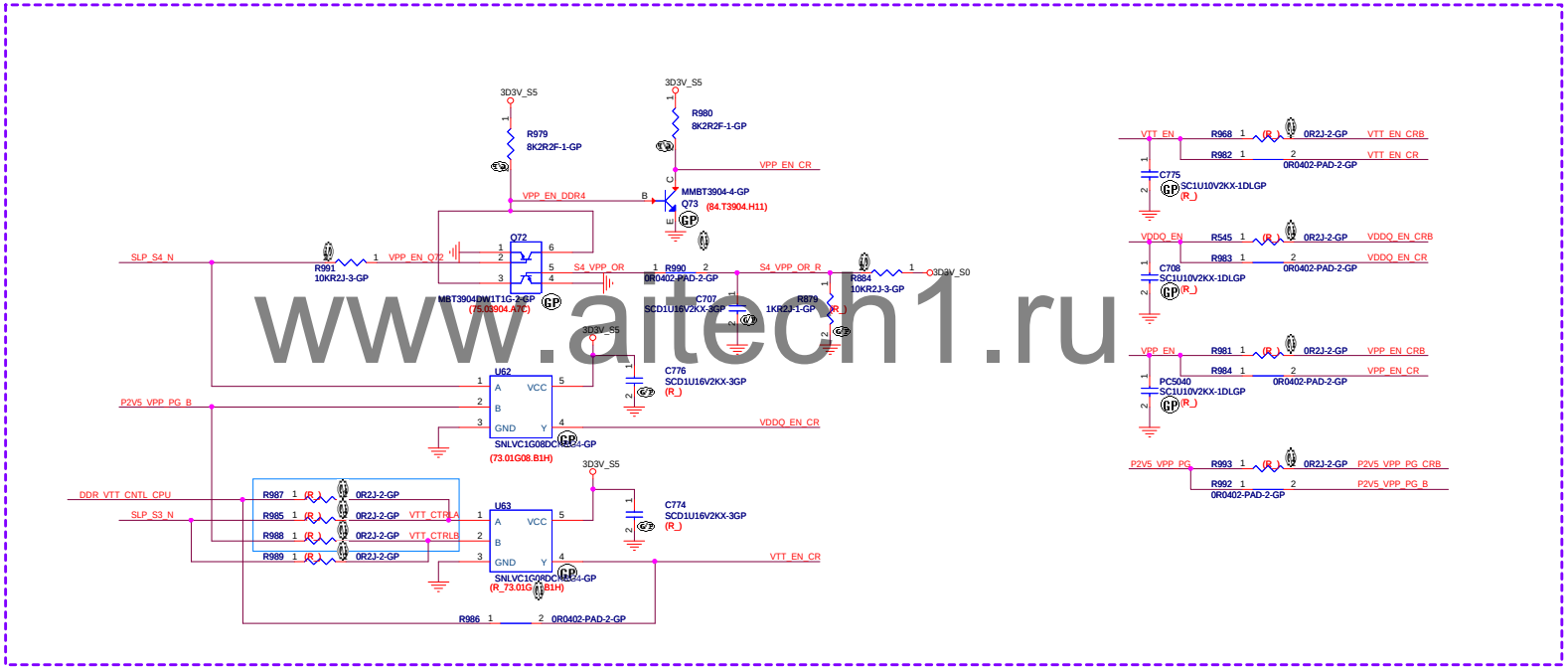

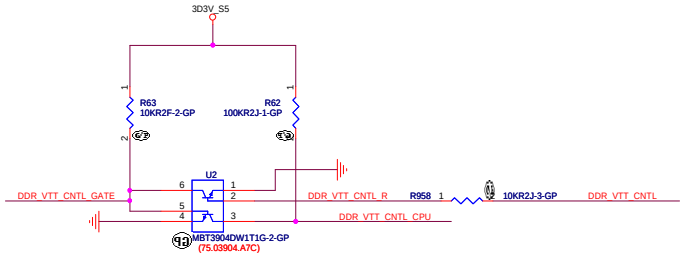

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Title: Power Sequence (DDR4)

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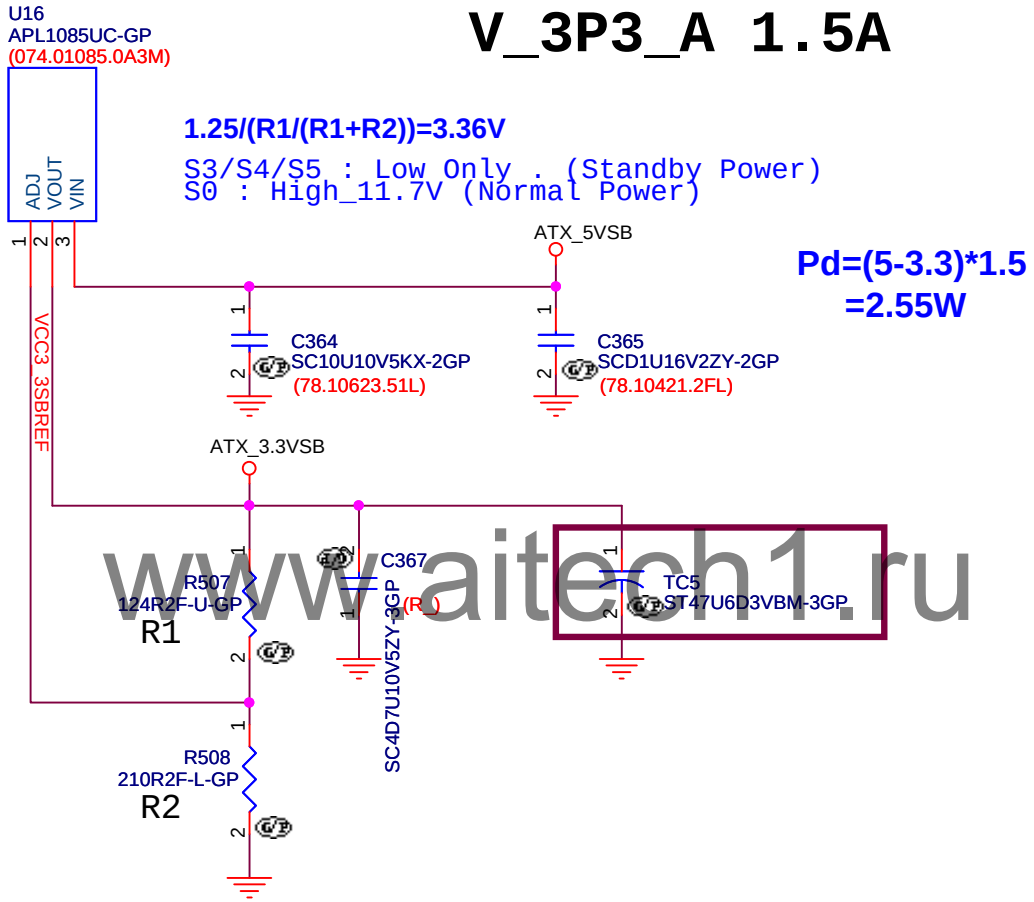
VCC5A/VCC3A

V_3P3_A 1.5A



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Title: DCDC-3D3V&5V		
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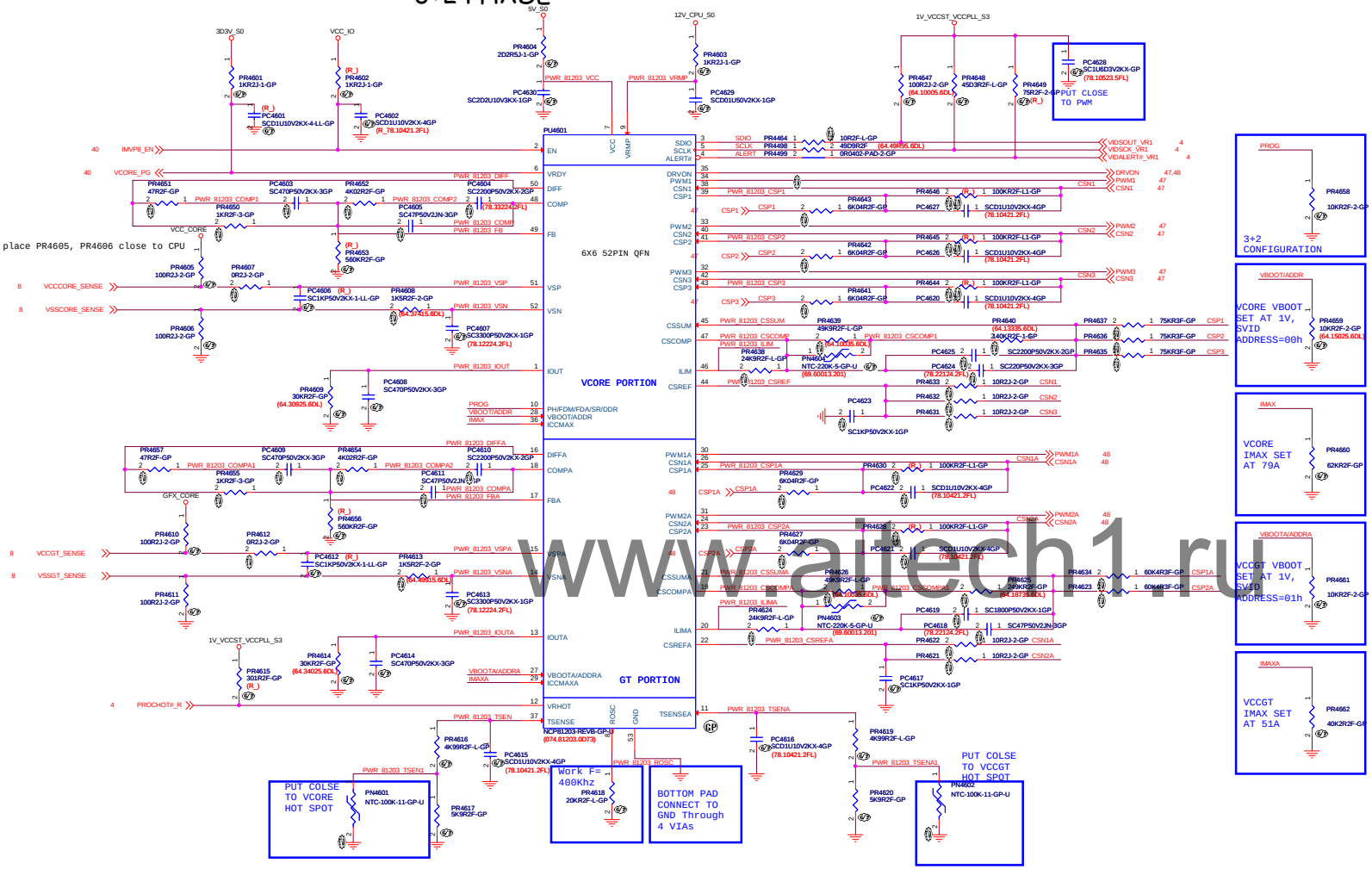
Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE



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<Core Design>

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Hsichih, Taipei Hsien

Title: VCORE & V_GT IC(NCP81203)

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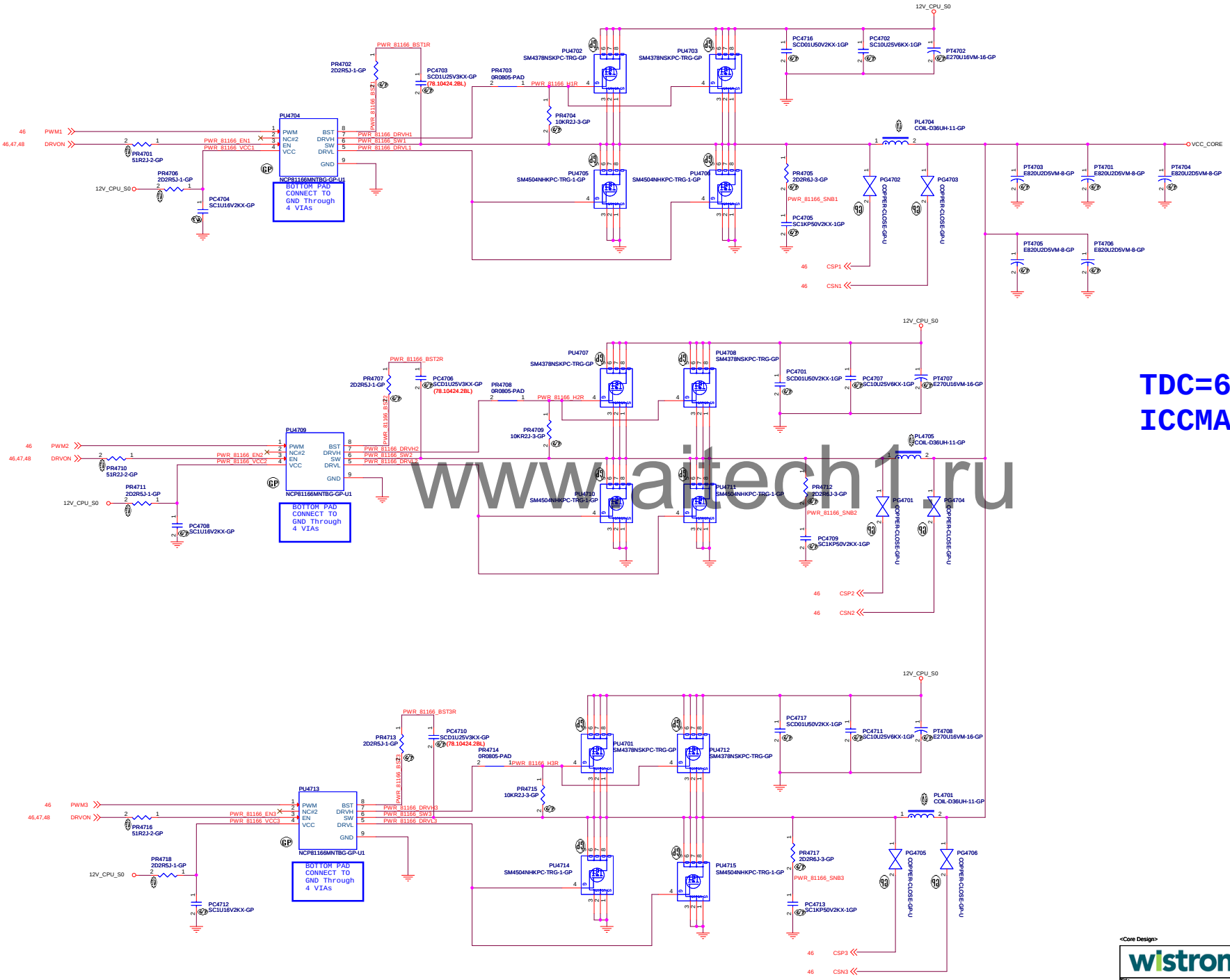
Vin ripple=10.48A



TDC=64A
ICCMAX=86A

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Title: VCORE OUTPUT (NCP81151)

Size: Custom | Document Number: vHulk | Rev: -1

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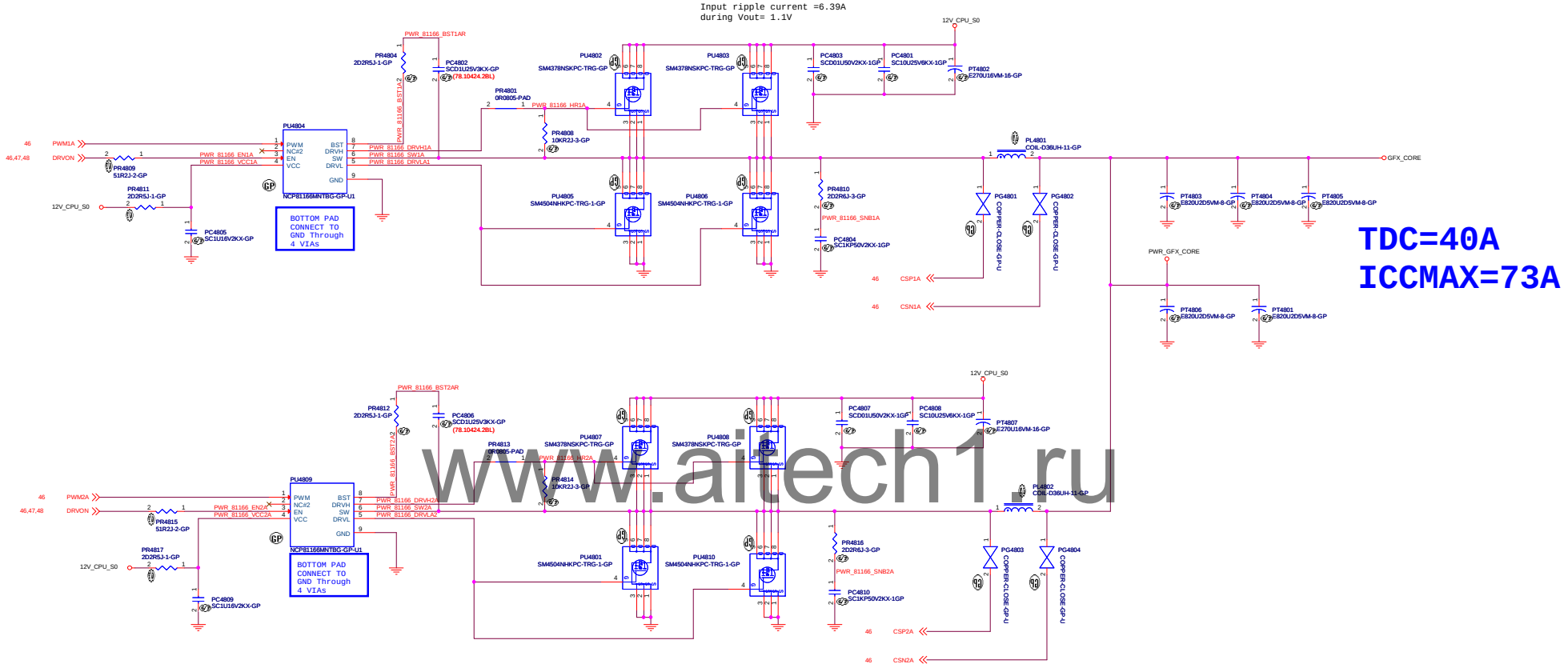

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Title: V_GT OUTPUT(NCP81151)

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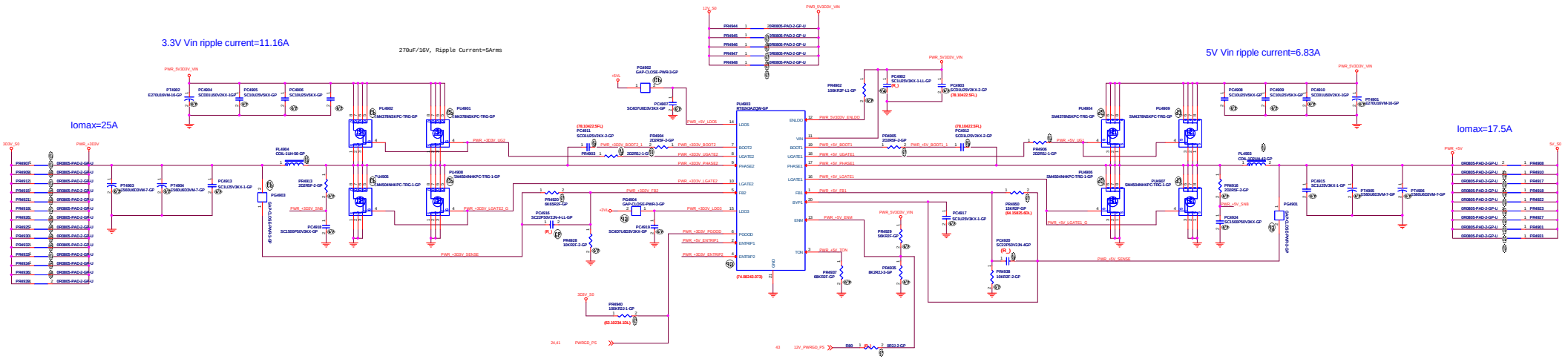
PWR_3D3V/PWR_5V



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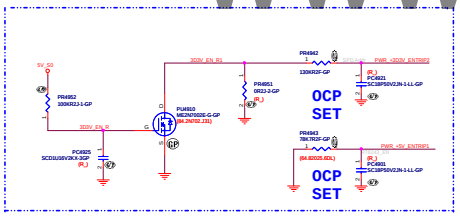

Table 2. Power Up Sequencing(RT8243A)

ENLDO(V)	SECFB	ENTRIP1	ENTRIP2	LDO5(V)	LDO3(V)	SMPS1	SMPS2
LOW	LOW	X	X	Off	Off	Off	Off
>1.6V =>High	LOW	X	X	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	Off	On	On	Off	Off
>1.6V =>High	>2.3V =>High	Off	On	On	On	Off	On
>1.6V =>High	>2.3V =>High	On=>PD	On=>PD	On	On	On	On
>1.6V =>High	>2.3V =>High	On	Off	On	On	On	On

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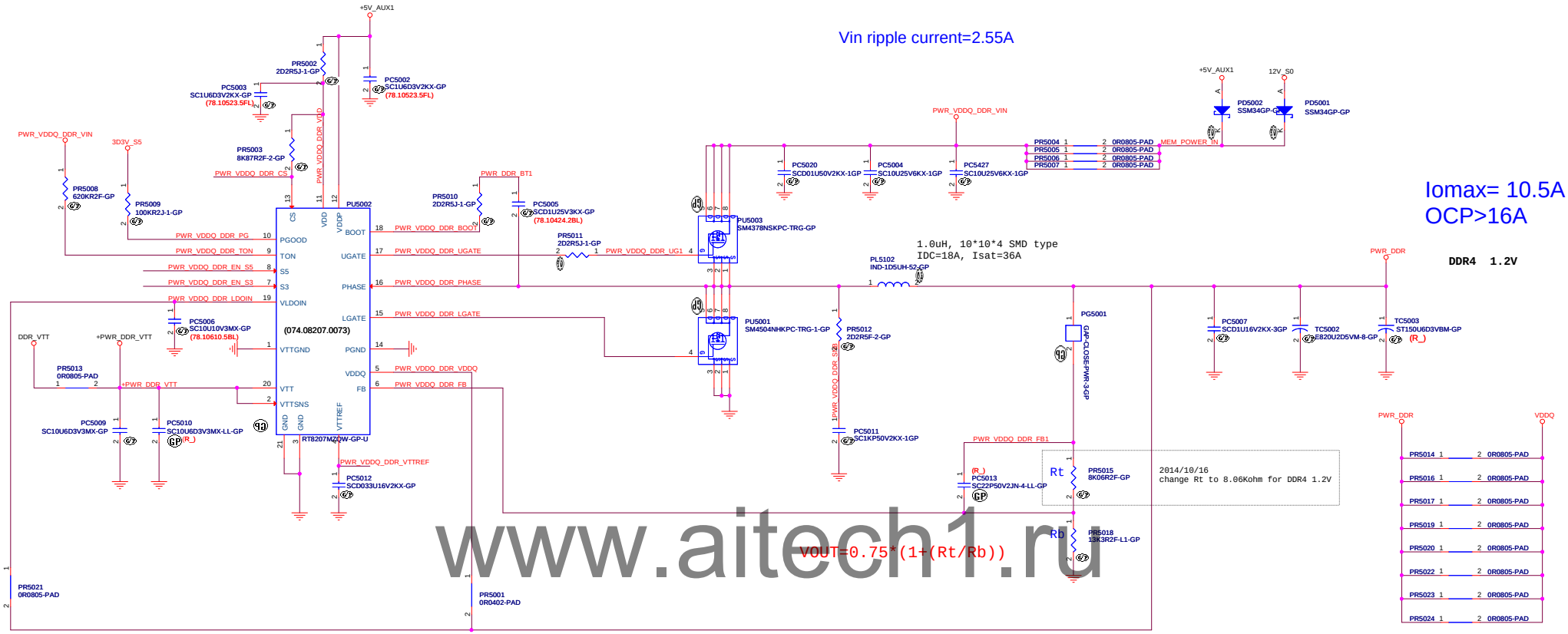
5V &3.3V(RT8243A)

Wednesday, September 23, 2015



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Title: DDR_PWR(RT8207M)

Size: Custom | Document Number: vHulk | Rev: -1

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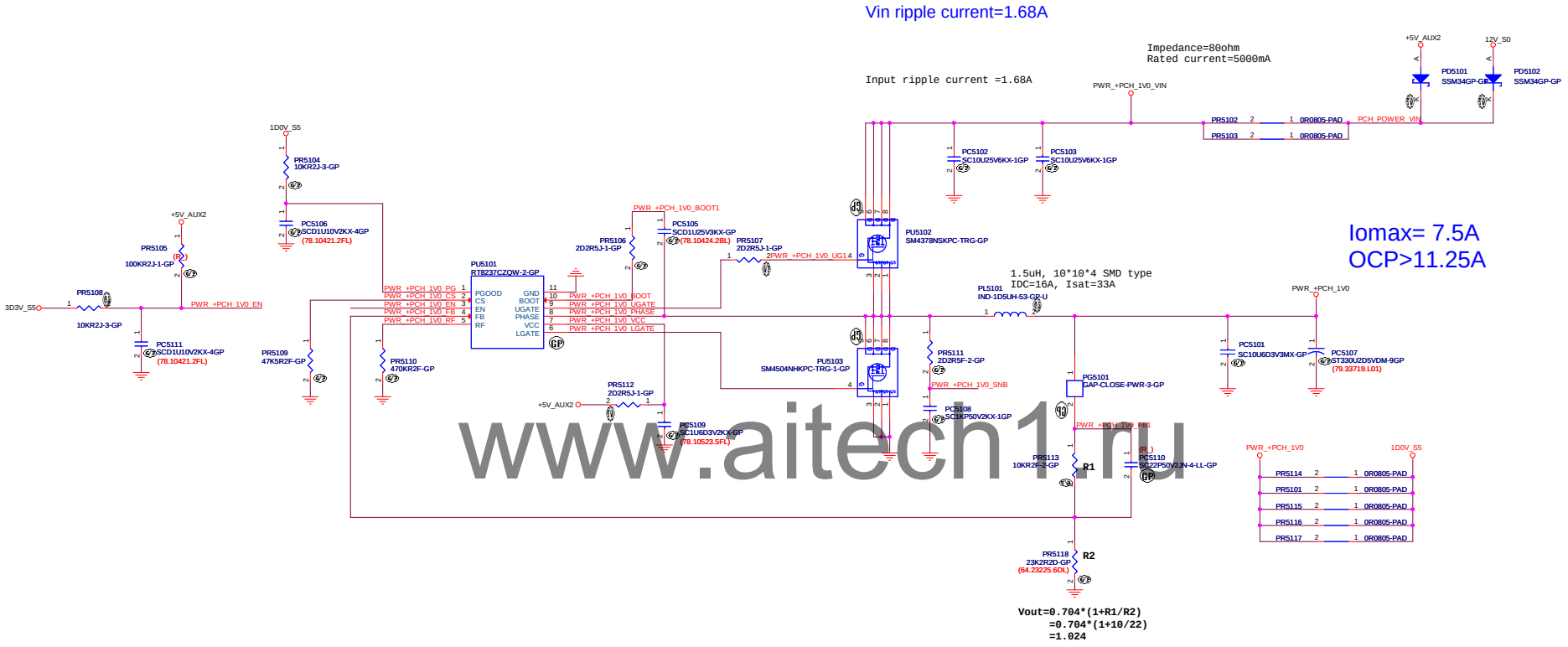

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Title: PCH_1P0V (RT8237C)

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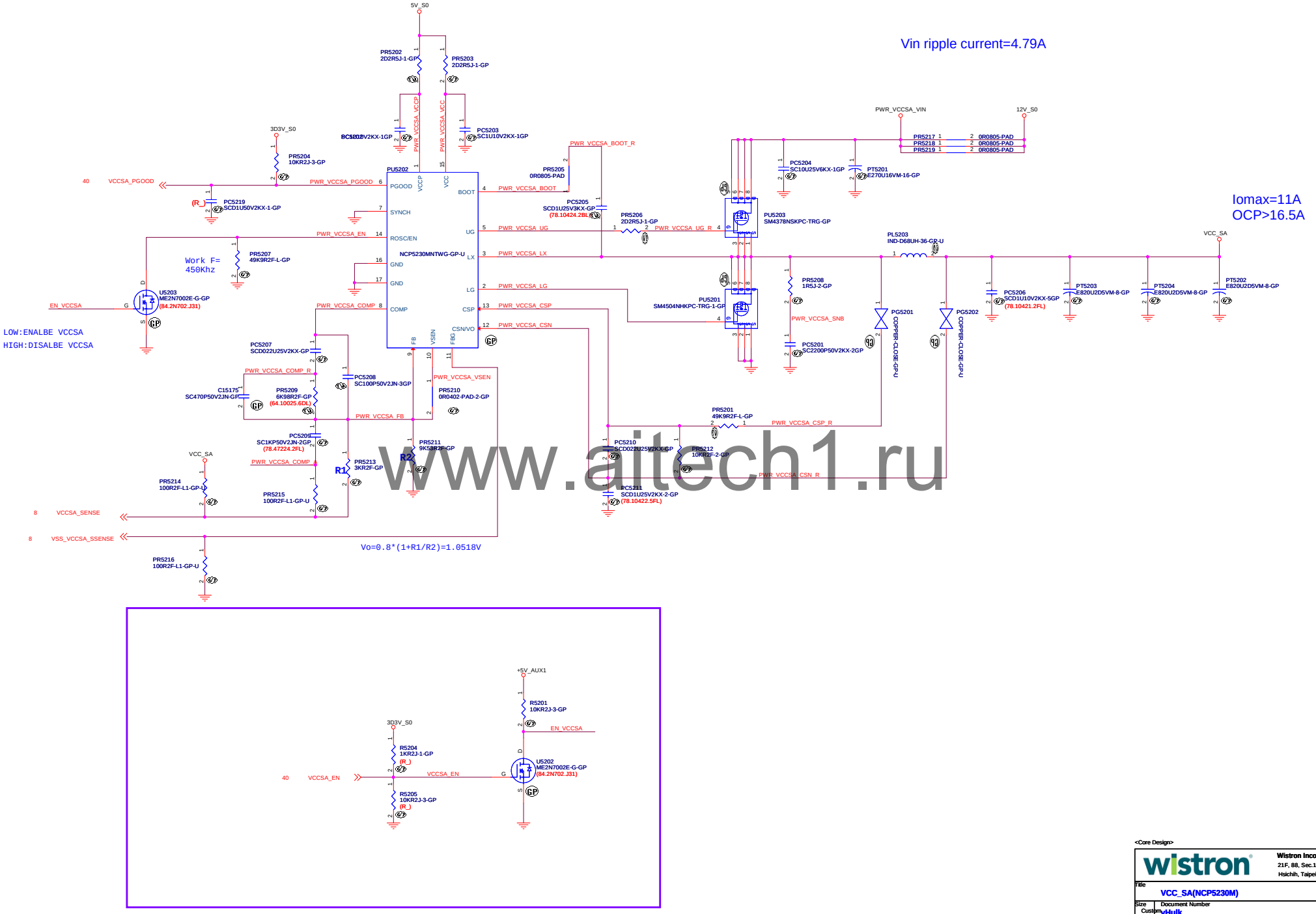

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Title: VCC_SA(NCP5230M)

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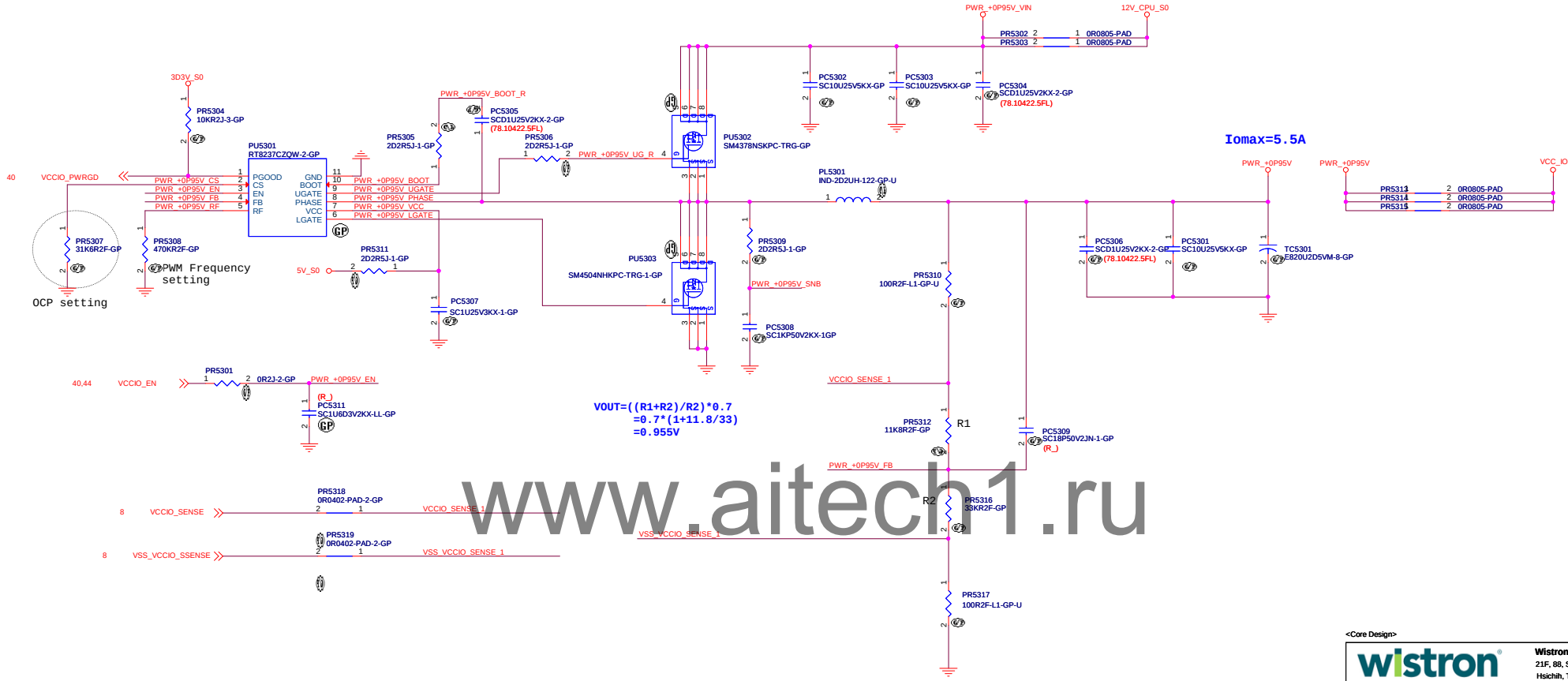
VCCIO



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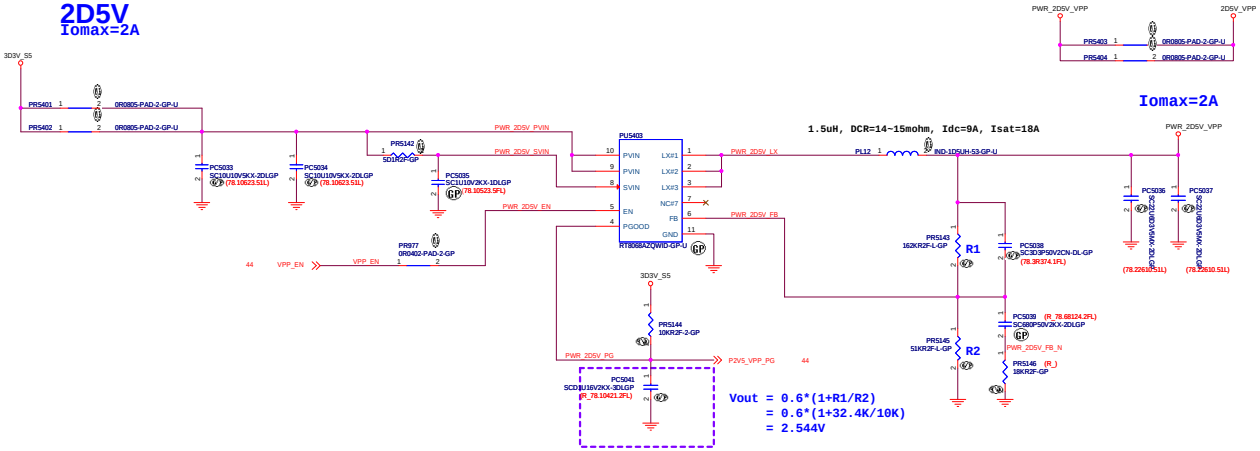
Date: Wednesday, September 23, 2015 | Sheet 53 of 107

VPP_2P5

2014/8/26
Del 1D5V_S0

2D5V
Iomax=2A



2014/8/26
Del 1D8V_S5

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Title: LDO_3P3A_1P5V_1P8V

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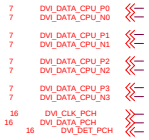
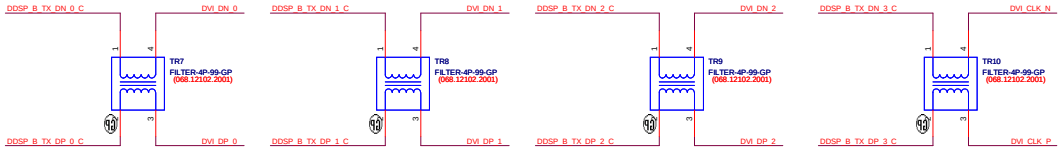
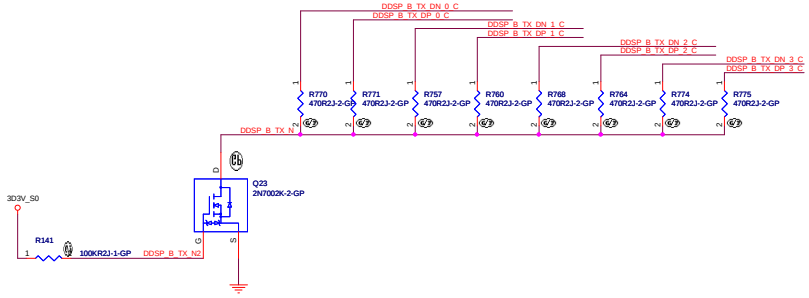
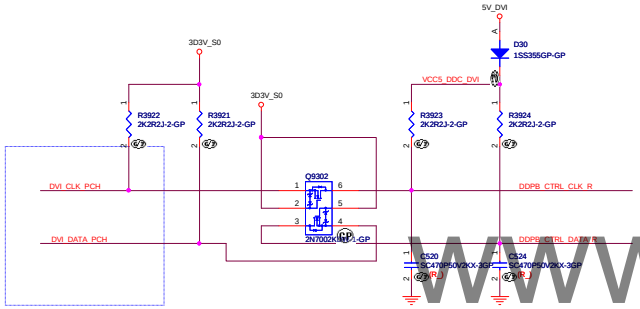
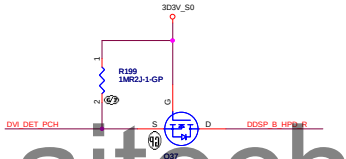
DDI PORT B

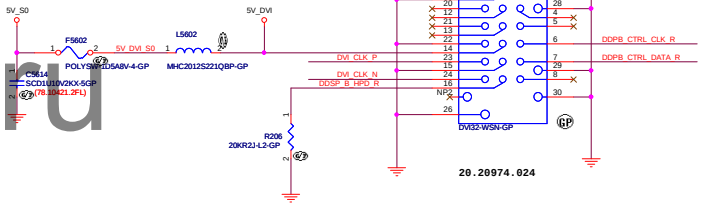






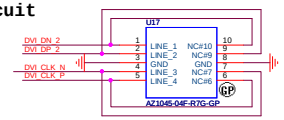


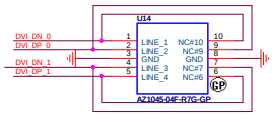


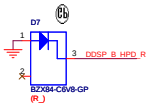


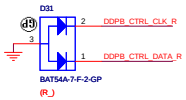
20.20974.024

ESD circuit









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7 DP2_DATA_CPU_P0
7 DP2_DATA_CPU_N0
7 DP2_DATA_CPU_P1
7 DP2_DATA_CPU_N1
7 DP2_DATA_CPU_P2
7 DP2_DATA_CPU_N2
7 DP2_DATA_CPU_P3
7 DP2_DATA_CPU_N3
7 DP2_AUX_CPU_N
7 DP2_AUX_CPU_P
16 DP2_CTRLCLK_PCH
16 DP2_CTRLDATA_PCH
16 DP2_HPD_PCH
24 DP2_PWR_CTRL

Place all CAP near DP Connector

DP2_DATA_CPU_P0 — C5720 1 2 SCD1U16V2KX-3GP — DP2_DATA_P0
DP2_DATA_CPU_N0 — C5715 1 2 SCD1U16V2KX-3GP — DP2_DATA_N0
DP2_DATA_CPU_P1 — C5723 1 2 SCD1U16V2KX-3GP — DP2_DATA_P1
DP2_DATA_CPU_N1 — C5718 1 2 SCD1U16V2KX-3GP — DP2_DATA_N1
DP2_DATA_CPU_P2 — C5719 1 2 SCD1U16V2KX-3GP — DP2_DATA_P2
DP2_DATA_CPU_N2 — C5725 1 2 SCD1U16V2KX-3GP — DP2_DATA_N2
DP2_DATA_CPU_P3 — C5726 1 2 SCD1U16V2KX-3GP — DP2_DATA_P3
DP2_DATA_CPU_N3 — C5722 1 2 SCD1U16V2KX-3GP — DP2_DATA_N3
DP2_AUX_CPU_N — C5724 1 2 SCD1U16V2KX-3GP — DP2_AUX_CPU_N_C
DP2_AUX_CPU_P — C5717 1 2 SCD1U16V2KX-3GP — DP2_AUX_CPU_P_C

3D3V_S0
DP2_PWR_CTRL — Q3109 AO3419L-GP (84.02130.031)
DP2PWR2
F5604 POLYSW-1D5A8V-4-GP
R5721 2 1 1MR2J-1-GP
30mil 500mA (Max.)
3D3V_DPPWR2_S0
C5714 SC470P50V2KX-3GP (R)
C5716 SCD1U16V2KX-3GP

DP connector

Impedance 85 ohm

DP2
DP2_DATA_CON_P0 — DP2_DATA_CON_N0 — DP2_DATA_CON_P1 — DP2_DATA_CON_N1 — DP2_DATA_CON_P2 — DP2_DATA_CON_N2 — DP2_DATA_CON_P3 — DP2_DATA_CON_N3 — DP2_Dongle_DET — DP2_AUX_CON_P — DP2_AUX_CON_N — DP2_HPD_CON
IN#1 IN#2 IN#3 IN#4 IN#6 IN#7 IN#9 IN#10 IN#12 CONFIG#13 CONFIG#14 I/O#15 I/O#17 OUT
GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND
RTN POWER_OUT
X1 X2 X3 X4
SKT-DISPLAY20P-25-GP
(022.10006.0101)

DP2_DATA_P0 — TR15 FILTER-4P-99-GP (68.00242.031) — DP2_DATA_CON_P0
DP2_DATA_N0 — DP2_DATA_CON_N0
DP2_DATA_P1 — TR16 FILTER-4P-99-GP (68.00242.031) — DP2_DATA_CON_P1
DP2_DATA_N1 — DP2_DATA_CON_N1
DP2_DATA_P2 — TR17 FILTER-4P-99-GP (68.00242.031) — DP2_DATA_CON_P2
DP2_DATA_N2 — DP2_DATA_CON_N2
DP2_DATA_P3 — TR18 FILTER-4P-99-GP (68.00242.031) — DP2_DATA_CON_P3
DP2_DATA_N3 — DP2_DATA_CON_N3

AUX

5V_S0
R5716 1KR2J-1-GP (R)
DP2_Dongle_DET — R5720 — 4K7R2J-2-GP — HDMI2_DEVICE_DETECT
R5726 1MR2J-1-GP
12V_S0
R5723 10KR2J-3-GP
HDMI2_Q64_PIN5 — (R) C5721 SC470P50V2KX-3GP
Q5706 MBT3904DW1T1G-2-GP
Q64_PIN2_R
DP2_DEVICE_DETECT
R5722 20KR2J-L2-GP
R5724 15KR2F-GP
R5717 4K99R2F-L-GP

3D3V_S0
R5725 2K2R2J-2-GP
DP2_CTRLCLK_PCH — HDMI2_DEVICE_DETECT — DP2_CTRLDATA_PCH
Q5705 2N7002KDW-1-GP
DP2_AUX_CON_P — HDMI2_DEVICE_DETECT — DP2_AUX_CON_N
R5718 2K2R2J-2-GP
3D3V_S0

3D3V_S0
R5728 100KR2J-1-GP
DP2_AUX_CON_N — DP2_DEVICE_DETECT — DP2_AUX_CPU_P_C
Q5707 2N7002KDW-1-GP
DP2_AUX_CPU_N_C — DP2_DEVICE_DETECT — DP2_AUX_CON_P
R5715 100KR2J-1-GP

HPD

5V_S0
R5727 100KR2J-3-GP (R)
DP2_HPD_PCH — Q5708 2N7002K-2-GP (84.05067.031) — DP2_HPD_CON
PLACE NEAR CONNECTOR PIN
R5719 100KR2J-1-GP

ESD

ED5706
DP2_DATA_CON_P2 — DP2_DATA_CON_N2 — DP2_DATA_CON_P3 — DP2_DATA_CON_N3
LINE_1 LINE_2 GND LINE_3 LINE_4 NC#10 NC#9 GND NC#7 NC#6
AZ1045-04F-R7G-GP

ED5705
DP2_DATA_CON_N1 — DP2_DATA_CON_P1 — DP2_DATA_CON_N0 — DP2_DATA_CON_P0
LINE_1 LINE_2 GND LINE_3 LINE_4 NC#10 NC#9 GND NC#7 NC#6
AZ1045-04F-R7G-GP

ED5704
DP2_Dongle_DET — DP2_AUX_CON_P — DP2_AUX_CON_N — DP2_HPD_CON
LINE_1 LINE_2 GND LINE_3 LINE_4 NC#10 NC#9 GND NC#7 NC#6
AZ1045-04F-R7G-GP

Display control line ESD Diodes

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7 DP_DATA_CPU_P0
7 DP_DATA_CPU_N0
7 DP_DATA_CPU_P1
7 DP_DATA_CPU_N1
7 DP_DATA_CPU_P2
7 DP_DATA_CPU_N2
7 DP_DATA_CPU_P3
7 DP_DATA_CPU_N3
7 DP_AUX_CPU_N
7 DP_AUX_CPU_P
16 DP_CTRLCLK_PCH
16 DP_CTRLDATA_PCH
16 DP_HPD_PCH
24 DP1_PWR_CTRL

Place all CAP near DP Connector

DP_DATA_CPU_P0 / DP_DATA_CPU_N0 — C5702 / C5703 SCD1U16V2KX-3GP — DP_DATA_P0 / DP_DATA_N0
DP_DATA_CPU_P1 / DP_DATA_CPU_N1 — C5704 / C5705 SCD1U16V2KX-3GP — DP_DATA_P1 / DP_DATA_N1
DP_DATA_CPU_P2 / DP_DATA_CPU_N2 — C5706 / C5707 SCD1U16V2KX-3GP — DP_DATA_P2 / DP_DATA_N2
DP_DATA_CPU_P3 / DP_DATA_CPU_N3 — C5708 / C5709 SCD1U16V2KX-3GP — DP_DATA_P3 / DP_DATA_N3
DP_AUX_CPU_N — C5710 SCD1U16V2KX-3GP — DP_AUX_CPU_N_C
DP_AUX_CPU_P — C5711 SCD1U16V2KX-3GP — DP_AUX_CPU_P_C

3D3V_S0
DP1_PWR_CTRL — Q3108 AO3419L-GP (84.02130.031)
DPPWR1
F5603 POLYSW-1D5A8V-4-GP
R5710 1MR2J-1-GP
30mil
500mA (Max.)
3D3V_DPPWR1_S0
C5712 SC470P50V2KX-3GP (R_)
C5713 SCD1U16V2KX-3GP

DP connector
Impedance 85 ohm

DP1 — SKT-DISPLAY20F-25-GP (022.10006.0101)
DP_DATA_CON_P0 / DP_DATA_CON_N0
DP_DATA_CON_P1 / DP_DATA_CON_N1
DP_DATA_CON_P2 / DP_DATA_CON_N2
DP_DATA_CON_P3 / DP_DATA_CON_N3
DP_Dongle_DET
DP1_14
DP_AUX_CON_P
DP_AUX_CON_N
DP_HPD_CON
CONFIG#13
CONFIG#14
I/O#15
I/O#17
GND
OUT
RTN
POWER_OUT

DP_DATA_P0 / DP_DATA_N0 — TR11 FILTER-4P-99-GP (S_68.00242.031,W_66.R0036.04L) — DP_DATA_CON_P0 / DP_DATA_CON_N0
DP_DATA_P1 / DP_DATA_N1 — TR12 FILTER-4P-99-GP (S_68.00242.031,W_66.R0036.04L) — DP_DATA_CON_P1 / DP_DATA_CON_N1
DP_DATA_P2 / DP_DATA_N2 — TR13 FILTER-4P-99-GP (S_68.00242.031,W_66.R0036.04L) — DP_DATA_CON_P2 / DP_DATA_CON_N2
DP_DATA_P3 / DP_DATA_N3 — TR14 FILTER-4P-99-GP (S_68.00242.031,W_66.R0036.04L) — DP_DATA_CON_P3 / DP_DATA_CON_N3

AUX

5V_S0
R5703 1KR2J-1-GP (R_)
12V_S0
R5704 10KR2J-3-GP
R5702 20KR2J-L-GP
R5705 15KR2F-GP
DP_Dongle_DET — R5707 4K7R2J-2-GP — HDMI_DEVICE_DETECT
HDMI_Q64_PIN5
Q5702 MBT3904DW1T1G-2-GP
Q64_PIN2
DP_DEVICE_DETECT
C5701 SC470P50V2KX-3GP (R_)
R5708 1MR2J-1-GP
R5709 4K99R2F-L-GP

3D3V_S0
R5711 2K2R2J-2-GP
DP_CTRLCLK_PCH
DP_CTRLDATA_PCH
HDMI_DEVICE_DETECT
Q5703 2N7002KDW-1-GP
DP_AUX_CON_P
DP_AUX_CON_N
R5713 2K2R2J-2-GP

3D3V_S0
R5712 100KR2J-1-GP
DP_AUX_CON_N
DP_DEVICE_DETECT
DP_AUX_CPU_P_C
Q5704 2N7002KDW-1-GP
DP_AUX_CPU_N_C
DP_AUX_CON_P
R5714 100KR2J-1-GP

HPD

5V_S0
R5701 100KR2J-1-GP (R_)
Q5701 2N7002K-2-GP (84.05067.031)
DP_HPD_PCH
DP_HPD_CON
PLACE NEAR CONNECTOR PIN
R5706 100KR2J-1-GP

ESD

ED5702 AZ1045-04F-R7G-GP
DP_DATA_CON_P2 / DP_DATA_CON_N2
DP_DATA_CON_P3 / DP_DATA_CON_N3

ED5703 AZ1045-04F-R7G-GP
DP_DATA_CON_N1 / DP_DATA_CON_P1
DP_DATA_CON_N0 / DP_DATA_CON_P0

Display control line ESD Diodes

ED5701 AZ1045-04F-R7G-GP
DP_Dongle_DET
DP_AUX_CON_P
DP_AUX_CON_N
DP_HPD_CON

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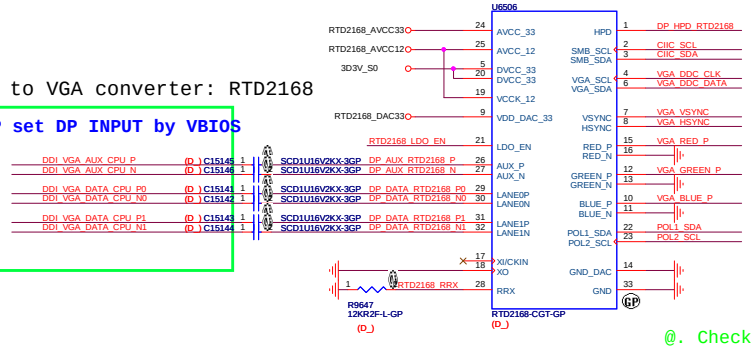
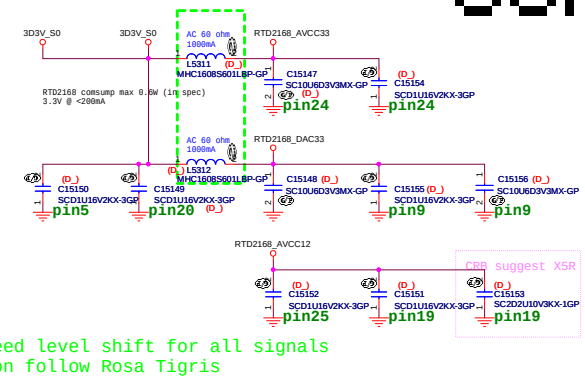
COMPRESSED IMAGE

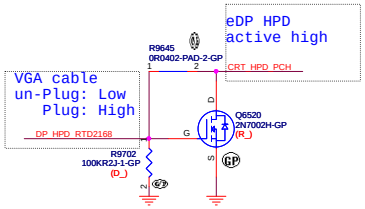
DP to VGA converter: RTD2168

DDI EDP set DP INPUT by VBIOS



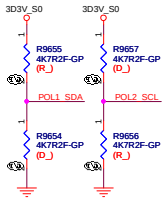
@. Check if need level shift for all signals
@. ESD solution follow Rosa Tigris





Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



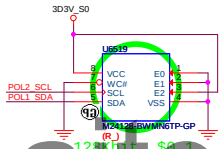
RTD2168 Supports three operation mode for system design. Reserve 4.7K resistor pull high/low for mode selection

ROM ONLY Mode: PIN22 pull low, PIN23 pull high
EP Mode : PIN22 pull high, PIN23 pull low
EEPROM Mode : PIN22 pull high, PIN23 pull high

EEPROM MODE

In EEPROM mode,an additional EEPROM is needed.
EEPROM should configure with following conditions.

1- EEPROM with a size of 16K-Byte
2- EEPROM device should be 2-byte addressing device
3- Slave address should configure as 0xA8



128Kbit $0.1 too expensive

I2C address=0xA8

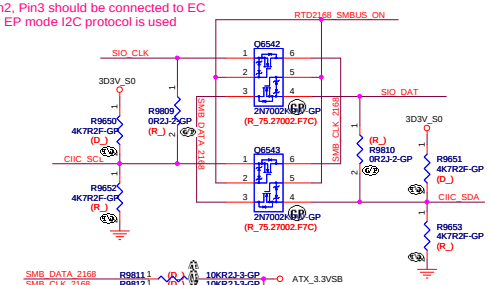
Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

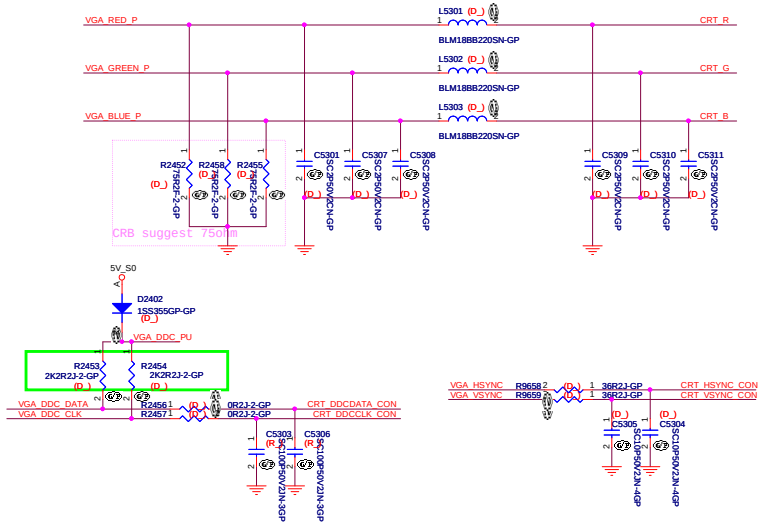
Select VCCK_V12 source from external 1.2V or embedded LDO

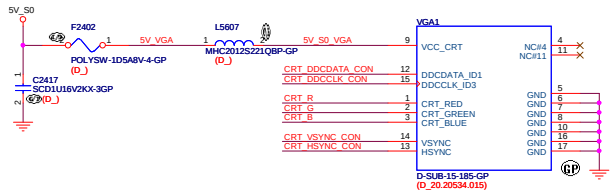
EP Mode

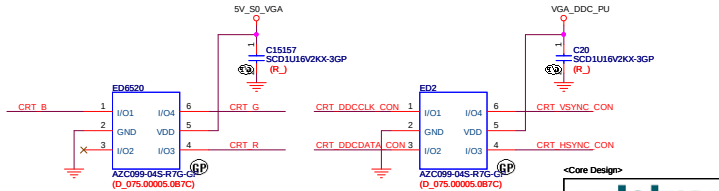
Pin2, Pin3 should be connected to EC for EP mode I2C protocol is used



RTD2168 Slave Address: 0x64/0x65







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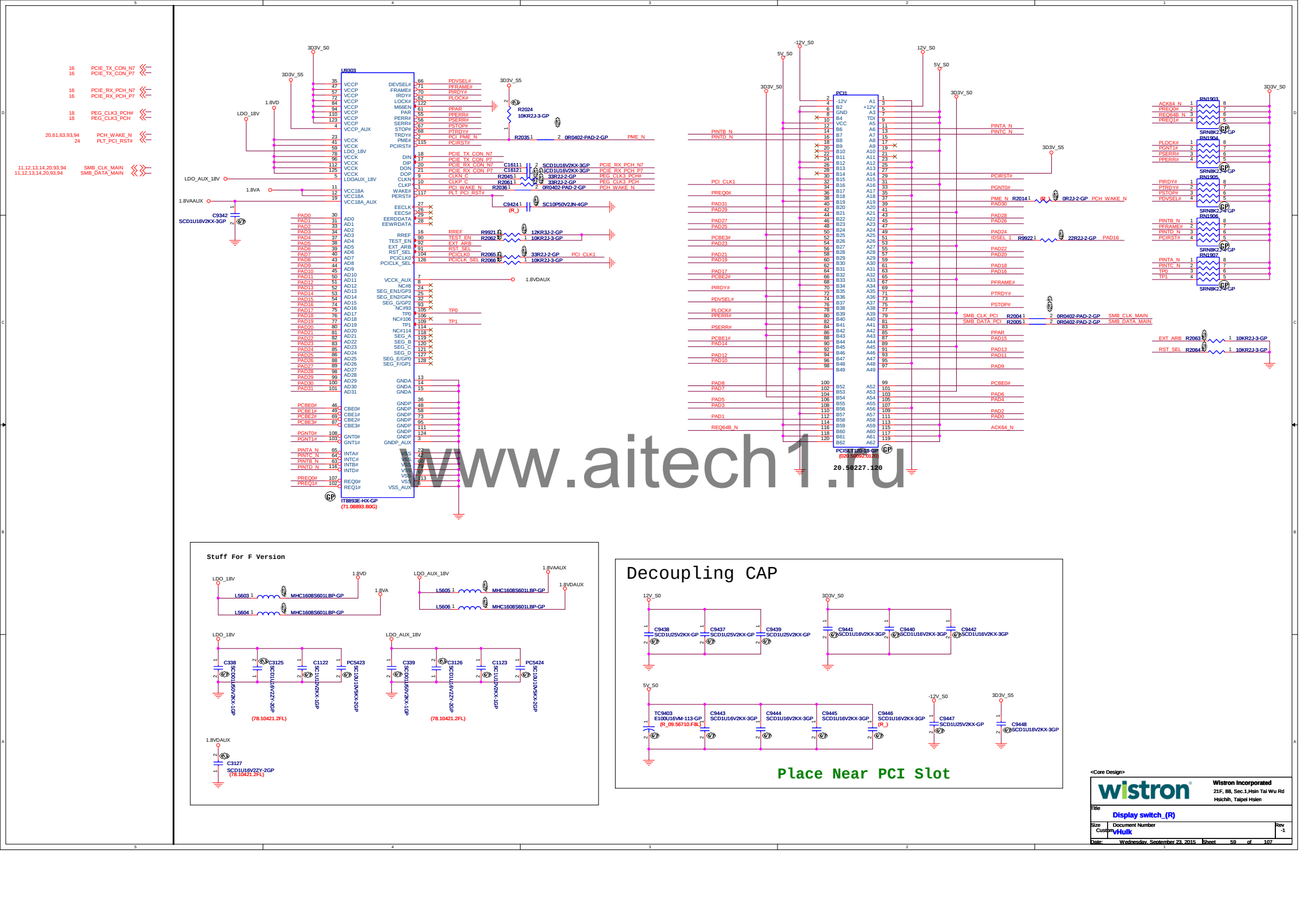

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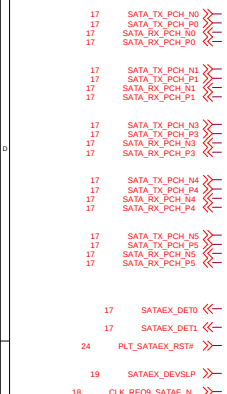
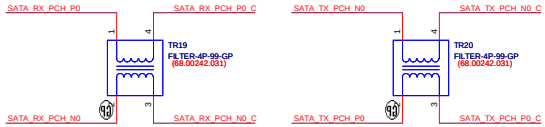
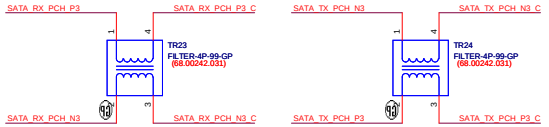
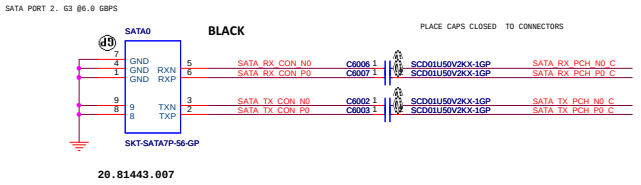
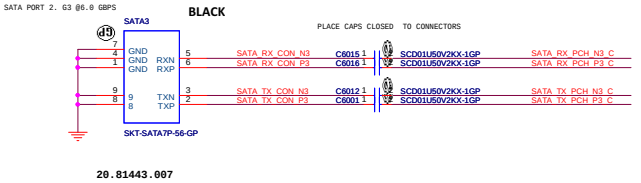
SATA Port

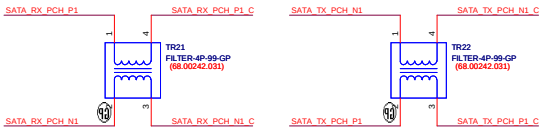


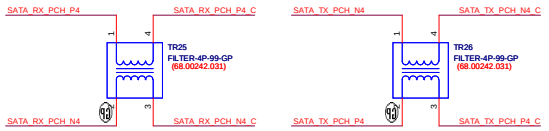


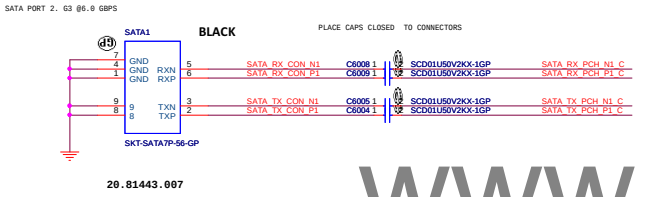


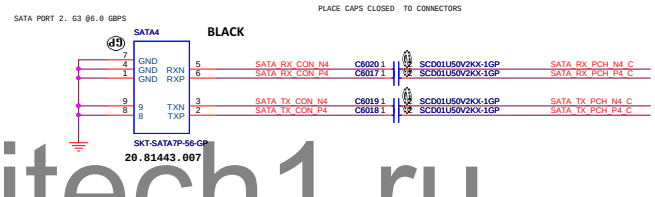












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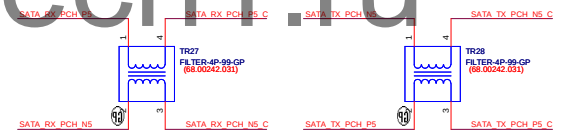
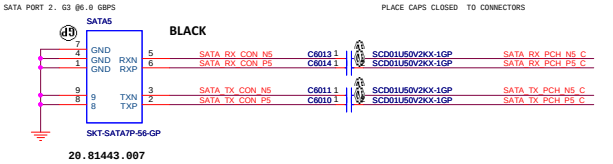
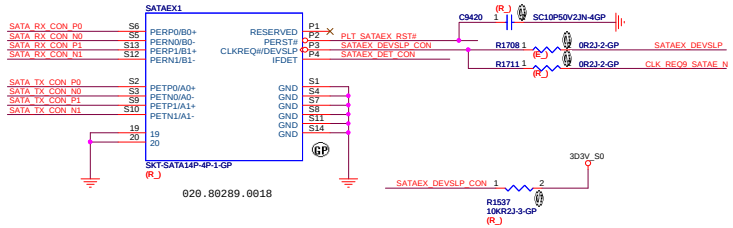
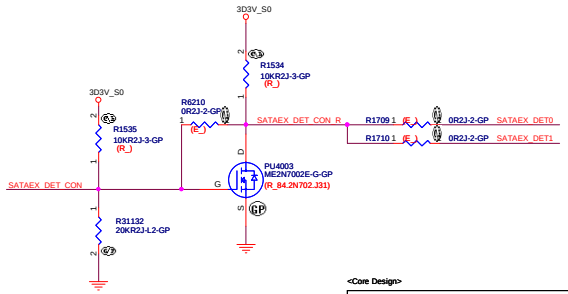
SATA Power Conn





SATA Express Port





<Core Design>
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Title: HDD/ODD
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M.2 2230 / 1630 Key E Type

USB

16 USB_PCH_PP12
16 USB_PCH_PN12

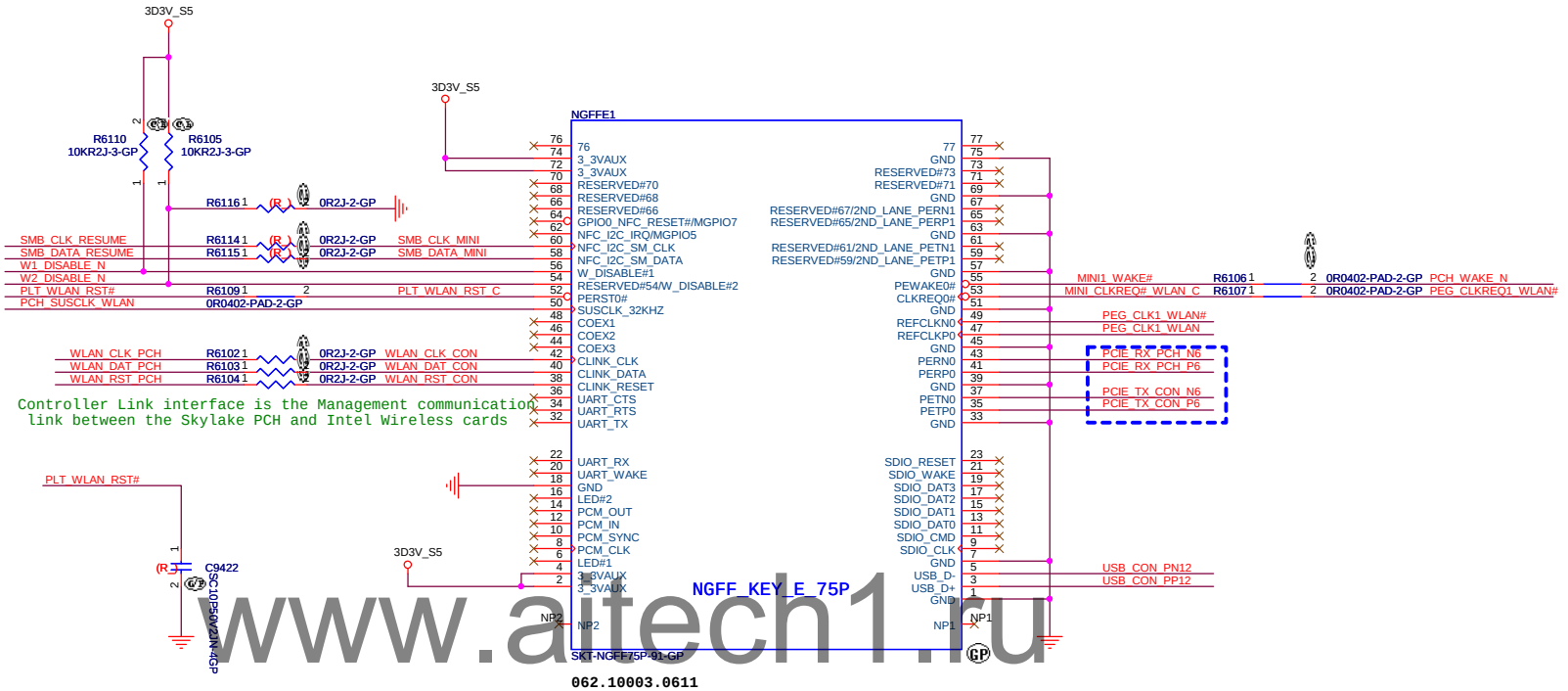
PCIEX1

16 PCIE_RX_PCH_N6
16 PCIE_RX_PCH_P6
16 PCIE_TX_CON_N6
16 PCIE_TX_CON_P6

18 PEG_CLK1_WLAN
18 PEG_CLK1_WLAN#

OTHERS

20,59,63,93,94 PCH_WAKE_N
24,61,63 PLT_WLAN_RST#
18 PEG_CLKREQ1_WLAN#
17 WLAN_RST_PCH
17 WLAN_DAT_PCH
17 WLAN_CLK_PCH
20 SMB_CLK_RESUME
20 SMB_DATA_RESUME
15 W1_DISABLE_N
15 W2_DISABLE_N
24,61,63 PLT_WLAN_RST#
20 PCH_SUSCLK_WLAN



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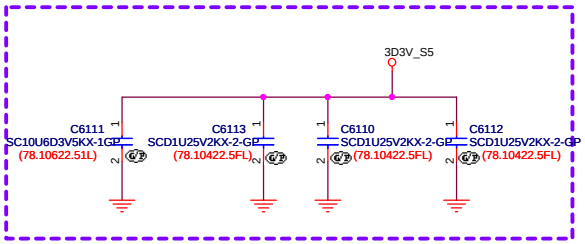
062.10003.0611

HS1
STF256R109H99-GP
(334.0350J.0001)
34.3NH01.001



<Core Design>

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Size: Custom | Document Number: vHulk | Rev: -1

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20 SUSCLK_PCH_M2

20,59,61,93,94 PCH_WAKE_N
18 PEG_CLKREQ0_M2#
24,61 PLT_WLAN_RST#

19 SSD_SATA_DEVSLP

17 M2_SATA_DET_PCH

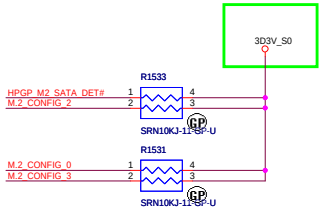
18 PEG_CLK0_M2
18 PEG_CLK0_M2#

17 SATA_TX_PCH_P2
17 SATA_TX_PCH_N2

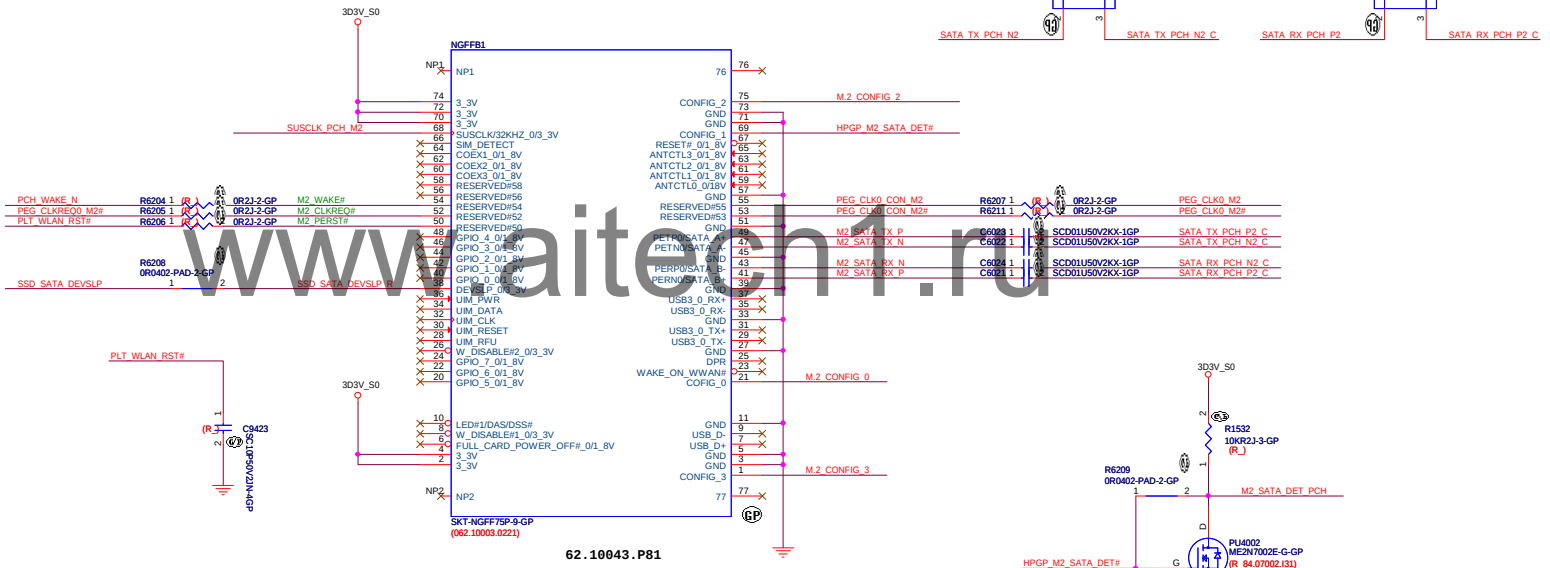
17 SATA_RX_PCH_P2
17 SATA_RX_PCH_N2

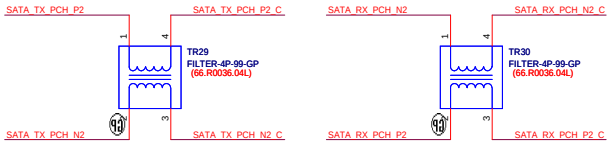
Table 46. Socket 2 Module Configuration Table

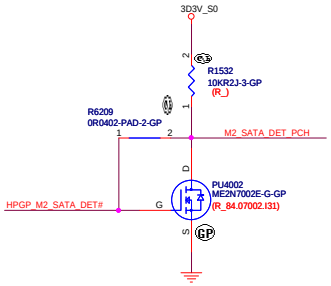
Module Configuration Decodes					
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A
0	0	1	0	WWAN - PCIe	0

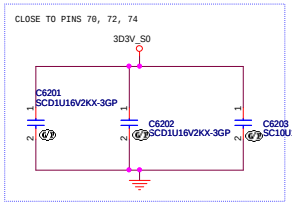


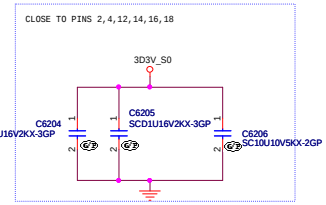
M.2 Key B Type











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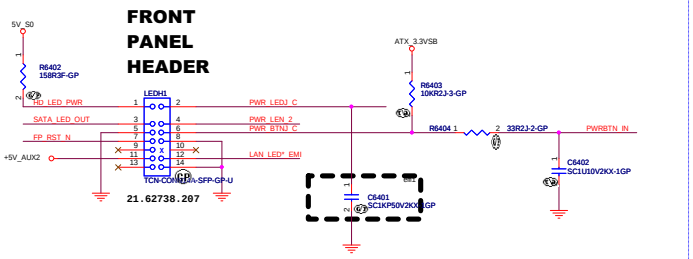
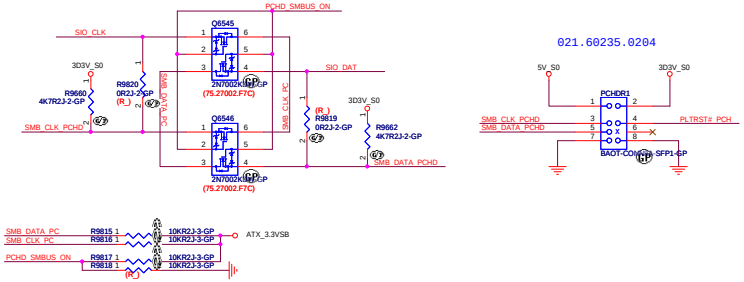
20 FP_RST_N
24 SUSLED_N
24,58 SIO_CLK
24,58 SIO_DAT
24 PWR_LEN_2_SIO
17 PCH_SATA_LED_N
24 PWRBTN_IN
24 PCHD_SMBUS_ON
15,24,68,91,97 PLTRST#_PCH
24 LAN_LED3_CTRL
31,32,97 LAN_LINKACTIVITY_LAN_N
24 TURN_OFF_PWM

FRONT PANEL HEADER

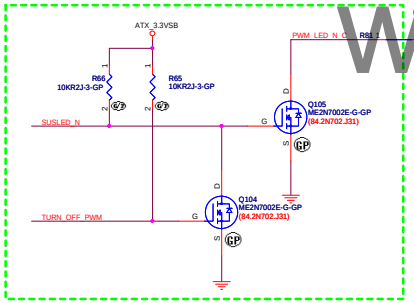


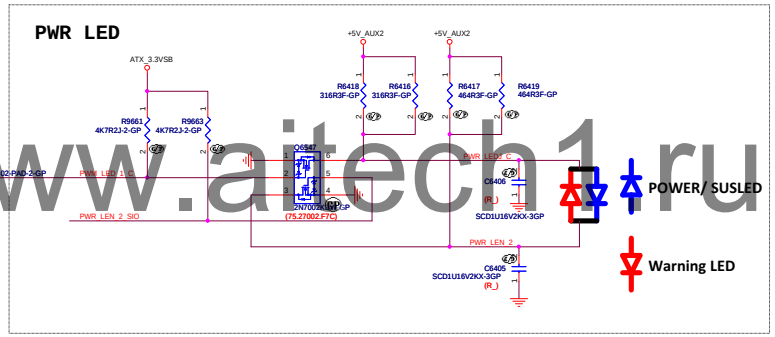
PC Health Header



	S0	S0 / Warning	S3	S3 / Warning	S4	S5
SUSLED_N	HIGH	LOW	H & L Circling (Blink)	LOW	HIGH	LOW
PWR_LEN_2_SIO	HIGH	H & L Circling (Blink)	HIGH	H & L Circling (Blink)	LOW	HIGH

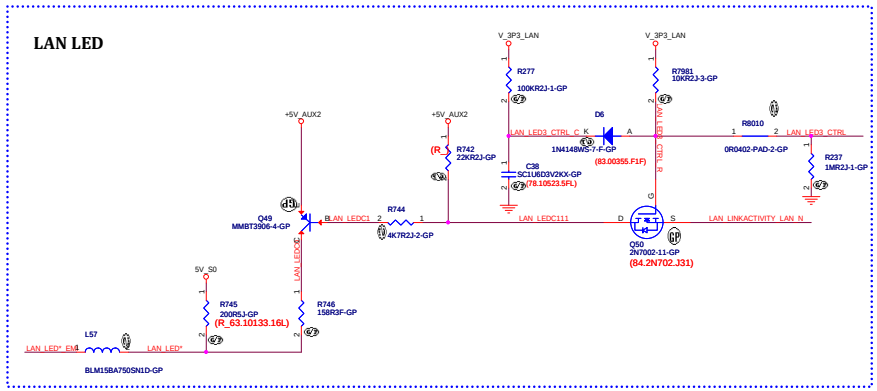
PWR LED



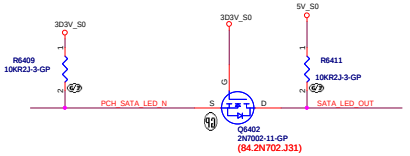


System State/Health	Indicator Behavior
S0/ Good *	Blue
S0/ Warning or	Blink Red
S3/ Good *	Blink Blue
S3/ Warning or	Blink Red
S4	No light
S5	No light

LAN LED



HDD LED



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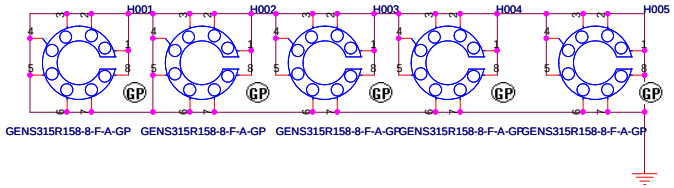

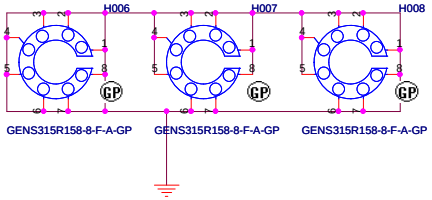

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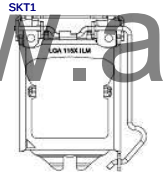
SKYLAKE SOCKET

SKT1

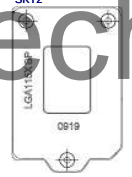


Load Plate
(22.78006.001)

Vendor: FOXCONN
P/N: 22.78006.001

Vendor: LOTES
P/N: 22.78005.181

SKT2

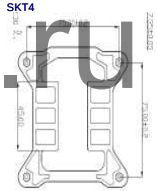


Back Plate
(22.78006.011)

Vendor: FOXCONN
P/N: 22.78006.011
Thickness:2.0mm (with mylar)

Vendor: LOTES
P/N: 022.70001.0121
Thickness: max 2.2mm (with mylar)

SKT4



ASSY BACK PLATE
(60.3EE01.002)
Thermal Component

SKT3

ILMCOVER
(22.78005.281)

Vendor: FOXCONN
P/N: 22.78005.281

Vendor: LOTES
P/N: 22.78005.171

LABEL

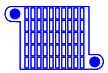
LBL1
LABEL
(40.3BZ24.011)
W30*H15

Battery Symbol

BAT1
BATTERY CR2032
(23.20068.001)

23.20068.001 KTS BBBCR2032BX
23.20023.311 MITSUBISHI CR2032 MITSUBISHI
23.22063.001 JHT CR2032 JHT

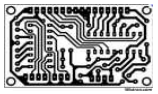
HeatSink Symbol



PCHHS1
HEATSINK
(60.3ET05.001)

Vendor
P/N:
60.3ET05.001
60.3ET05.021

PCB Symbol



PCB
PCB
(348.02802.0011)

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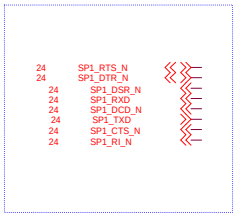
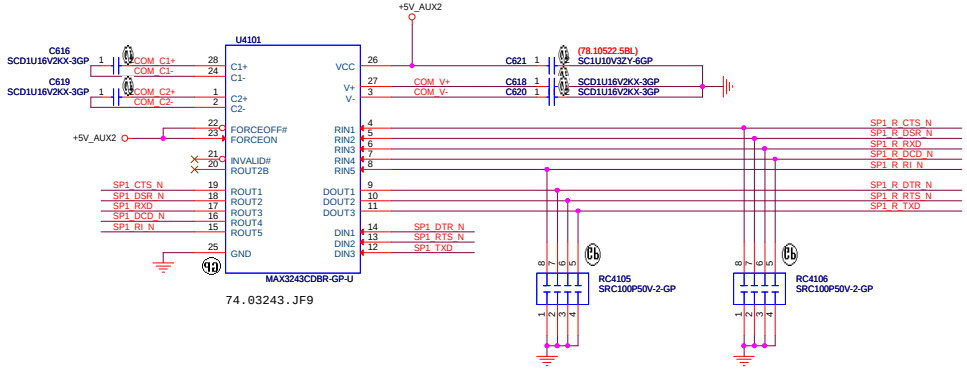
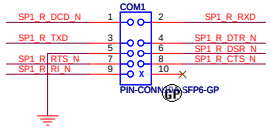
COM1



SERIAL PORT



COM port header



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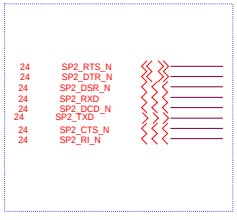
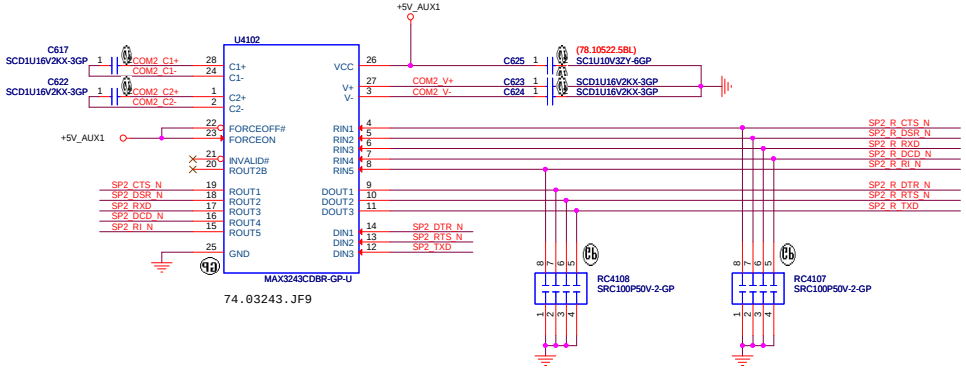
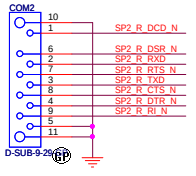
COM2



SERIAL PORT





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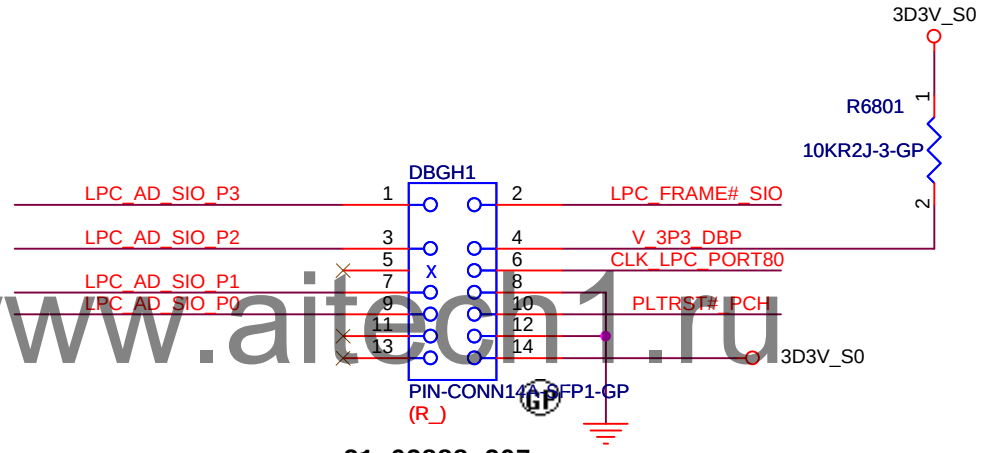
19,24,91 LPC_AD_SIO_P3
19,24,91 LPC_AD_SIO_P2
19,24,91 LPC_AD_SIO_P1
19,24,91 LPC_AD_SIO_P0

19,24,91 LPC_FRAME#_SIO

19,91 CLK_LPC_PORT80
15,24,64,91,97 PLTRST#_PCH

80 port

Layout close to SIO



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Annie pin define

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Title: Debug

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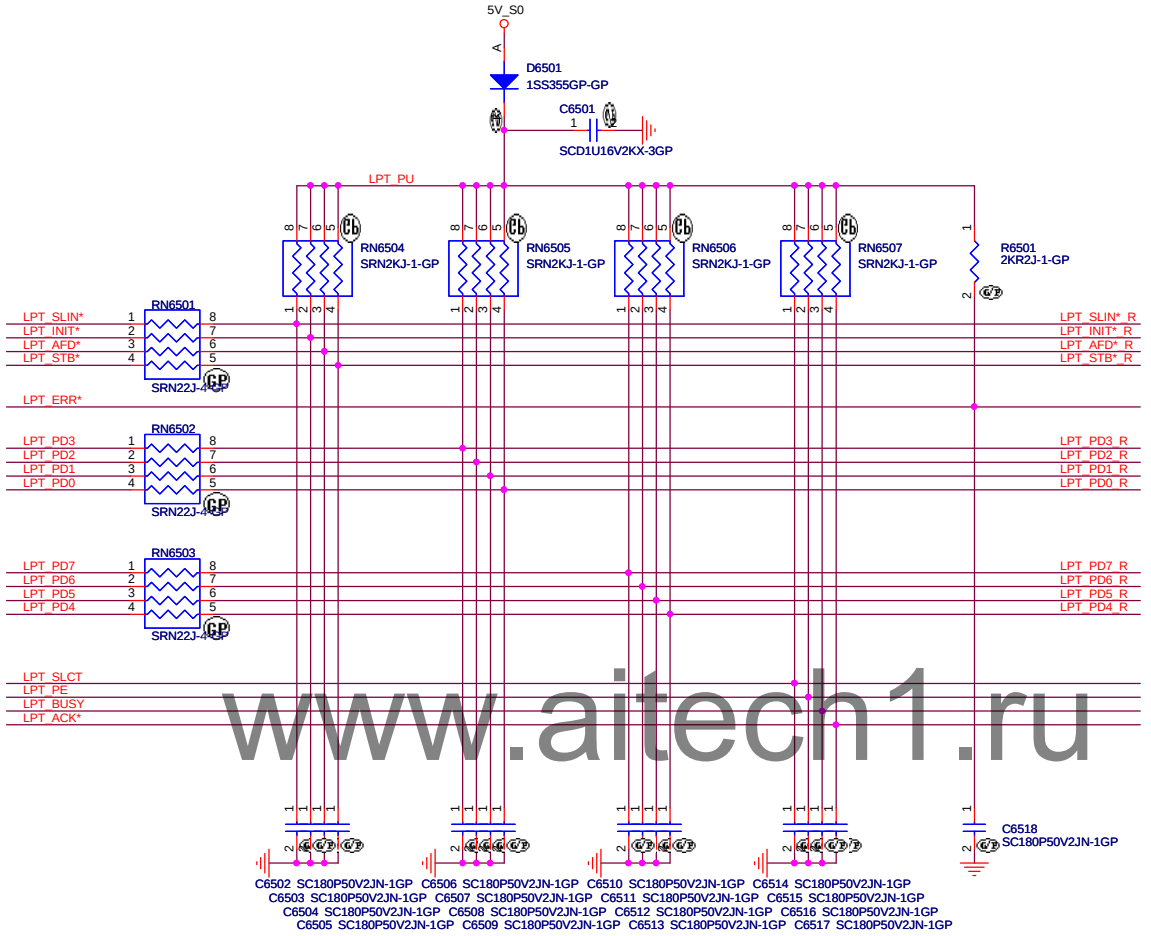
PARALLEL PORT

24 LPT_SLCT
24 LPT_PE
24 LPT_BUSY
24 LPT_ACK*
24 LPT_SLIN*
24 LPT_ERR*
24 LPT_AFD*
24 LPT_STB*
24 LPT_INIT*
24 LPT_PD[7:0]



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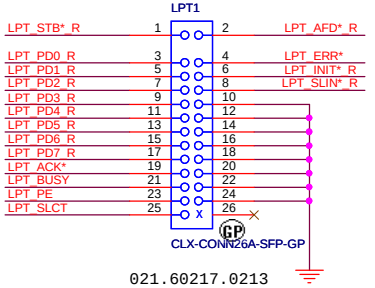
LPT



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Title: G sensor_(R)

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Title: Thunderbolt_(R)

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Title: GPU_(R)

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Title: GPU_(R)

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Title: GPU_(R)

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Title: GPU_(R)

Size	Document Number	Rev
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Title: GPU VRAM 1&2_(R)

Size	Document Number	Rev
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Title: GPU VRAM 3&4_(R)

Size	Document Number	Rev
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Title: GPU VRAM 5&6_(R)

Size	Document Number	Rev
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Title: GPU VRAM 7&8_(R)

Size	Document Number	Rev
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Title: GPU CORE_(R)

Size	Document Number	Rev
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Title: GPU discrete power_(R)

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Title: GPU Switch_(R)

Size: C | Document Number: vHulk | Rev: -1

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Title: GPU Switch_(R)

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Title: GPU Others_(R)

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Title: NFC_(R)

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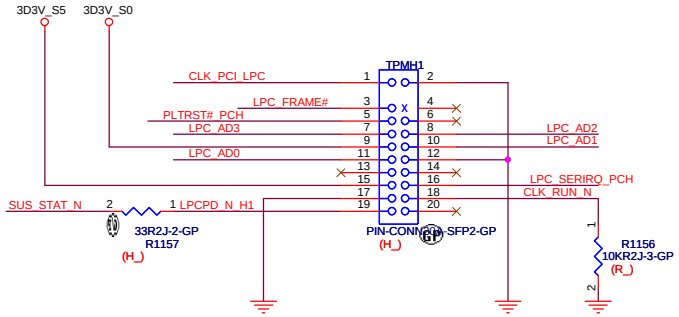
19,24,68 LPC_FRAME#_SIO — LPC_FRAME#
19,68 CLK_LPC_PORT80 — CLK_PCI_LPC
15,24,64,68,97 PLTRST#_PCH — PLTRST#_PCH
19,24,68 LPC_AD_SIO_P3 — LPC_AD3
19,24,68 LPC_AD_SIO_P2 — LPC_AD2
19,24,68 LPC_AD_SIO_P1 — LPC_AD1
19,24,68 LPC_AD_SIO_P0 — LPC_AD0
19 SUS_STAT_N
19,24 LPC_SERIRQ_PCH

TPM 2.54 pitch Header



TPM onboard chip for Q170

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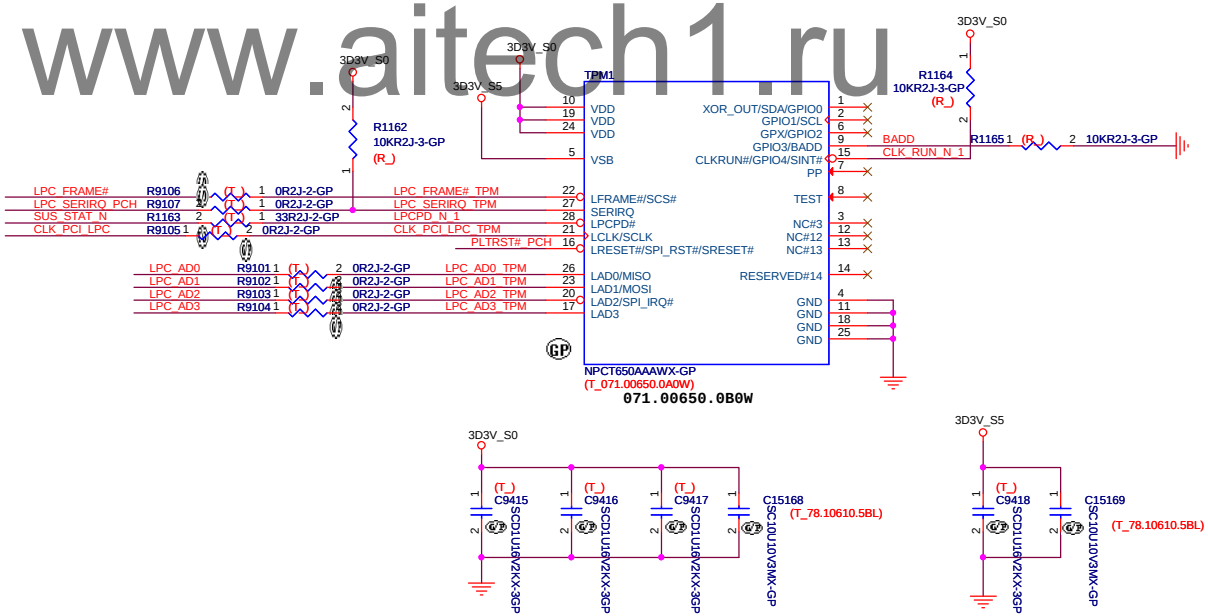

<Core Design>

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Title: TPM

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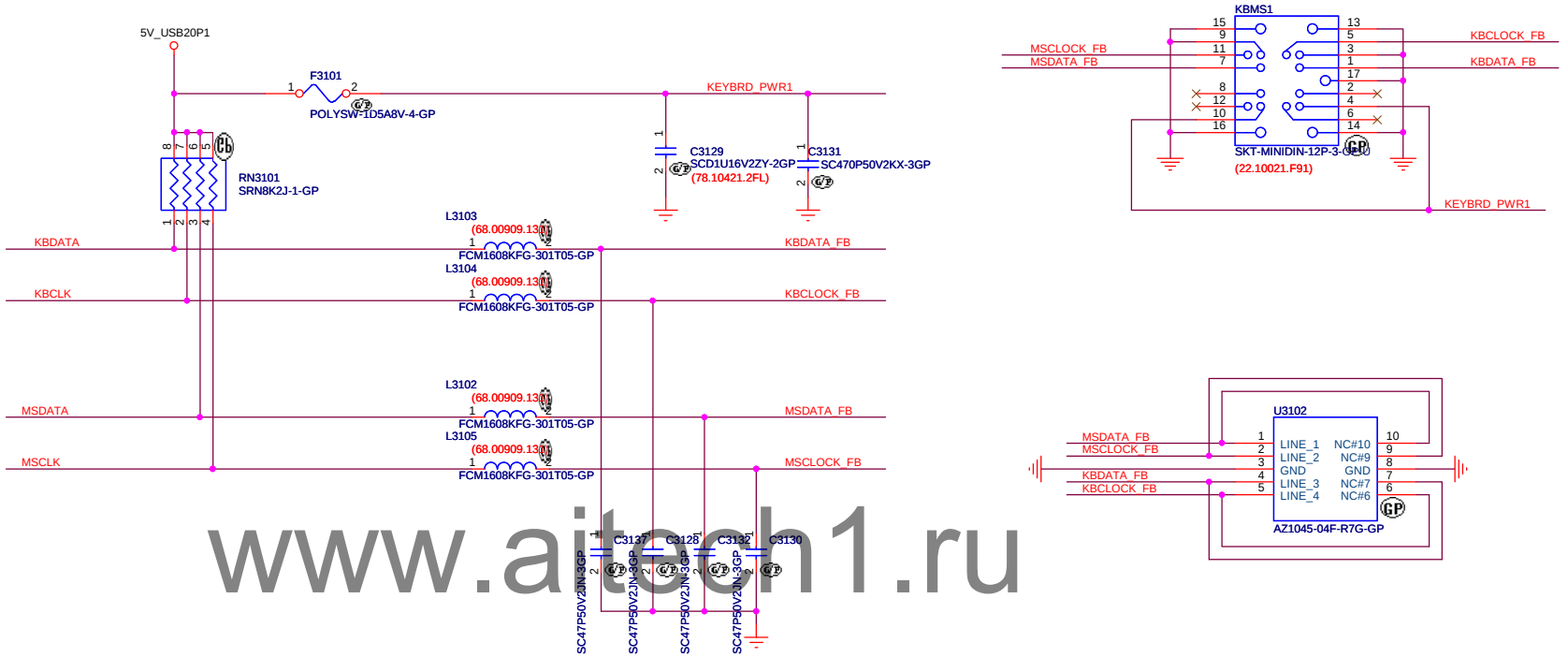
24 KBDATA
24 KBCLK
24 MSDATA
24 MSCLK



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Title: PS2

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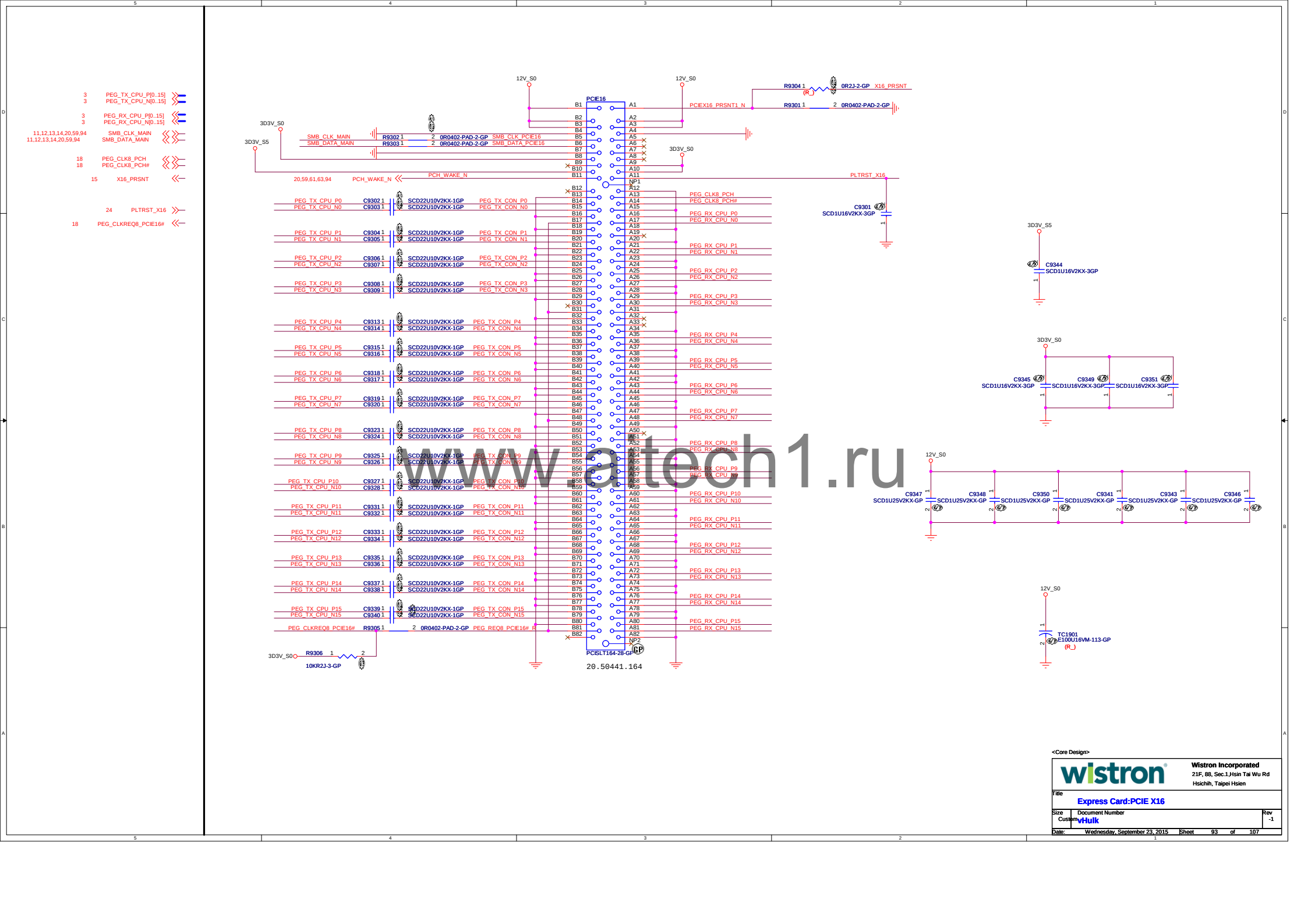

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Title: Express Card:PCIE X16

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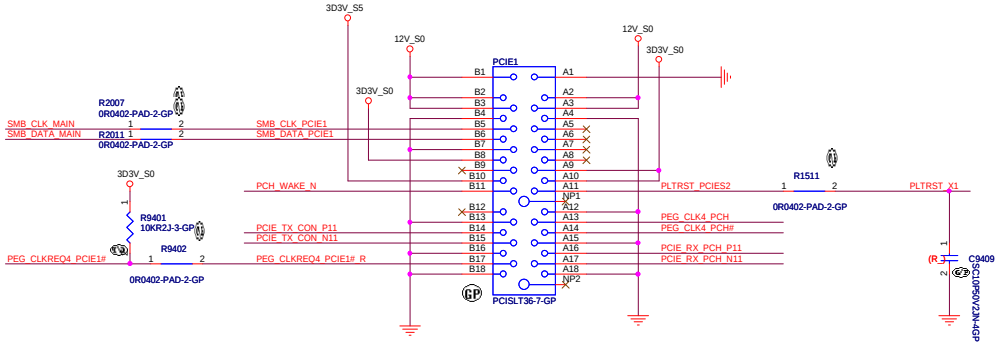
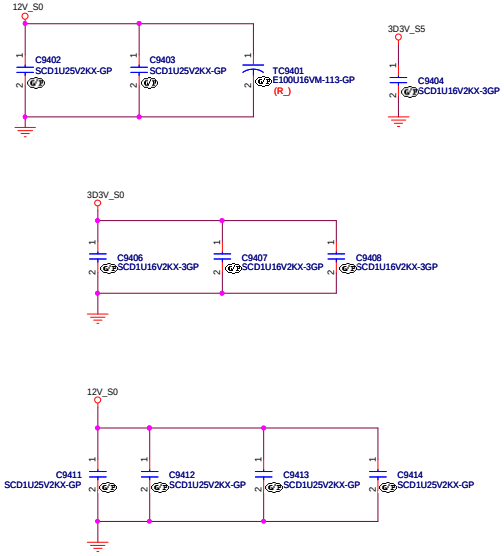
11,12,13,14,20,59,93 SMB_CLK_MAIN
11,12,13,14,20,59,93 SMB_DATA_MAIN
24 PLTRST_X1
20,59,61,63,93,94 PCH_WAKE_N
17 PCIE_TX_CON_P11
17 PCIE_TX_CON_N11
17 PCIE_RX_PCH_P11
17 PCIE_RX_PCH_N11
18 PEG_CLK4_PCH
18 PEG_CLK4_PCH#
18 PEG_CLKREQ4_PCIE1#

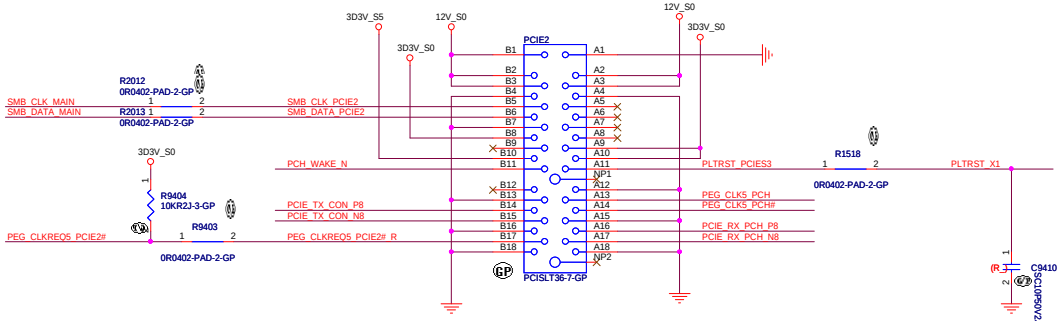
PCIEX1 CONN

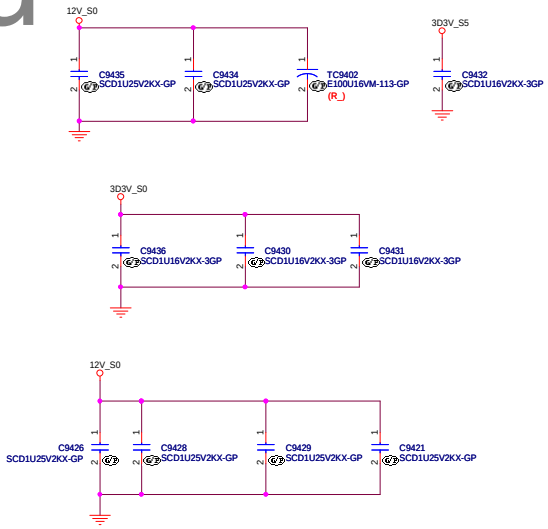




20,59,61,63,93,94 PCH_WAKE_N
16 PCIE_TX_CON_P8
16 PCIE_TX_CON_N8
16 PCIE_RX_PCH_P8
16 PCIE_RX_PCH_N8
18 PEG_CLK5_PCH
18 PEG_CLK5_PCH#
18 PEG_CLKREQ5_PCIE2#

PCIEX1 CONN





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Title: Smart Card PCIE X1
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Title: Scalar_(R)

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Title: MCU_(R)

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PCIE

18,31 PEG_CLK2_LAN
18,31 PEG_CLK2_LAN#
16,31 PCIE_TX_LAN_P5
16,31 PCIE_TX_LAN_N5
16,31 PCIE_RX_LAN_P5
16,31 PCIE_RX_LAN_N5

OTHERS

20 LAN_DISABLE_N
20 SMLINK0_CLK
20 SMLINK0_DATA
15,24,64,68,91 PLTRST#_PCH
24,31 LANWAKE_N
18,31 PEG_CLKREQ2_LAN#

31,32 LAN_MDI_LAN_P0
31,32 LAN_MDI_LAN_N0
31,32 LAN_MDI_LAN_P1
31,32 LAN_MDI_LAN_N1
31,32 LAN_MDI_LAN_P2
31,32 LAN_MDI_LAN_N2
31,32 LAN_MDI_LAN_P3
31,32 LAN_MDI_LAN_N3
31,32,97 LAN_SPEED1000_LAN_N
31,32,97 LAN_SPEED100_LAN_N
31,32,64,97 LAN_LINKACTIVITY_LAN_N
24 LAN_EN_PWR_SIO

If CLK_REQ_N is connected to PCIECLKRQ[1:2]#,the CLK_REQ_N pull-up resistor should be connected to +V3.3S.

LAN_MDI_P / LAN_MDI_N routing guide line: 4 mils on 10 mils spacing
Pair to pair should keep away with 25 mils

Place near Pin5

0.9Vdc
Keep short and wide

Q170: 1219-LM -->KI.JKV01.LM1

0.9Vdc POWER OPTIONS

Internal SRV	Shared with PCH's 1.05V SVR
LA36 : STUFF	LA36 : NO STUFF
RA1020 : NO STUFF	RA1020 : STUFF
R968 : STUFF	R968 : NO STUFF
RA886 : NO STUFF	RA886 : STUFF

10Mb: Green
100Mb: Green
1Gb: Orange
Active: Yellow Light flash

*NOTE: Clarkville has 0.9V internal SVR. However it is also possible to disable this 0.9V iSVR and Clarkville can support the external 1.05V supply (example sharing from PCH's 1.05V SVR). When sharing, make sure the 1.05V_SHARED is controlled by the SLP_LAN signal. Both +3.3V_LAN and 1.05V_SHARED rails are remained powered on during ALL Sx states, as required to support WOL.

LAN Power

AO3419 PMOS 3.5A

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Title: Intel LAN
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Title: LAN Switch_(R)

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XDP for CPU

4 H_PREQ_N
4 H_PRDY_N
4 SKL_PCUSTB_0_DP
4 SKL_PCUSTB_0_DN
4 BPM_CPU_N0
4 BPM_CPU_N1
4 SKL_PCUSTB_1_DP
4 SKL_PCUSTB_1_DN

20,24 PM_PWRBTN#

20,40 PCH_SYSPWROK

18 XDP_CLK_CON
18 XDP_CLK_CON#

4 CFG[0..15]

4 H_TCK
4 H_TDO
4 H_TDI
4 H_TMS
4 H_TRST_N

15,22,25 SPI_WP_PCH
4 XDP_PCUDEBUG<3>

XDP for CPU

XDP_PCUDEBUG<3>

H_PREQ_N
H_PRDY_N

CFG0
CFG1

CFG2
CFG3

BPM_CPU_N0
BPM_CPU_N1

CFG4
CFG5

CFG6
CFG7

H_TCK

SKL_PCUSTB_0_DP
SKL_PCUSTB_0_DN

CFG8
CFG9

CFG10
CFG11

SKL_PCUSTB_1_DP
SKL_PCUSTB_1_DN

CFG12
CFG13

CFG14
CFG15

XDP_CLK_CON
XDP_CLK_CON#

H_TDO
H_TRST_N
H_TDI
H_TMS

SPI_WP_CON R9914 1 2 SPI_WP_PCH
0R0402-PAD-2-GP

R9916
0R2J-2-GP

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Title: XDP&ITP

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Title
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Title: GPIO table

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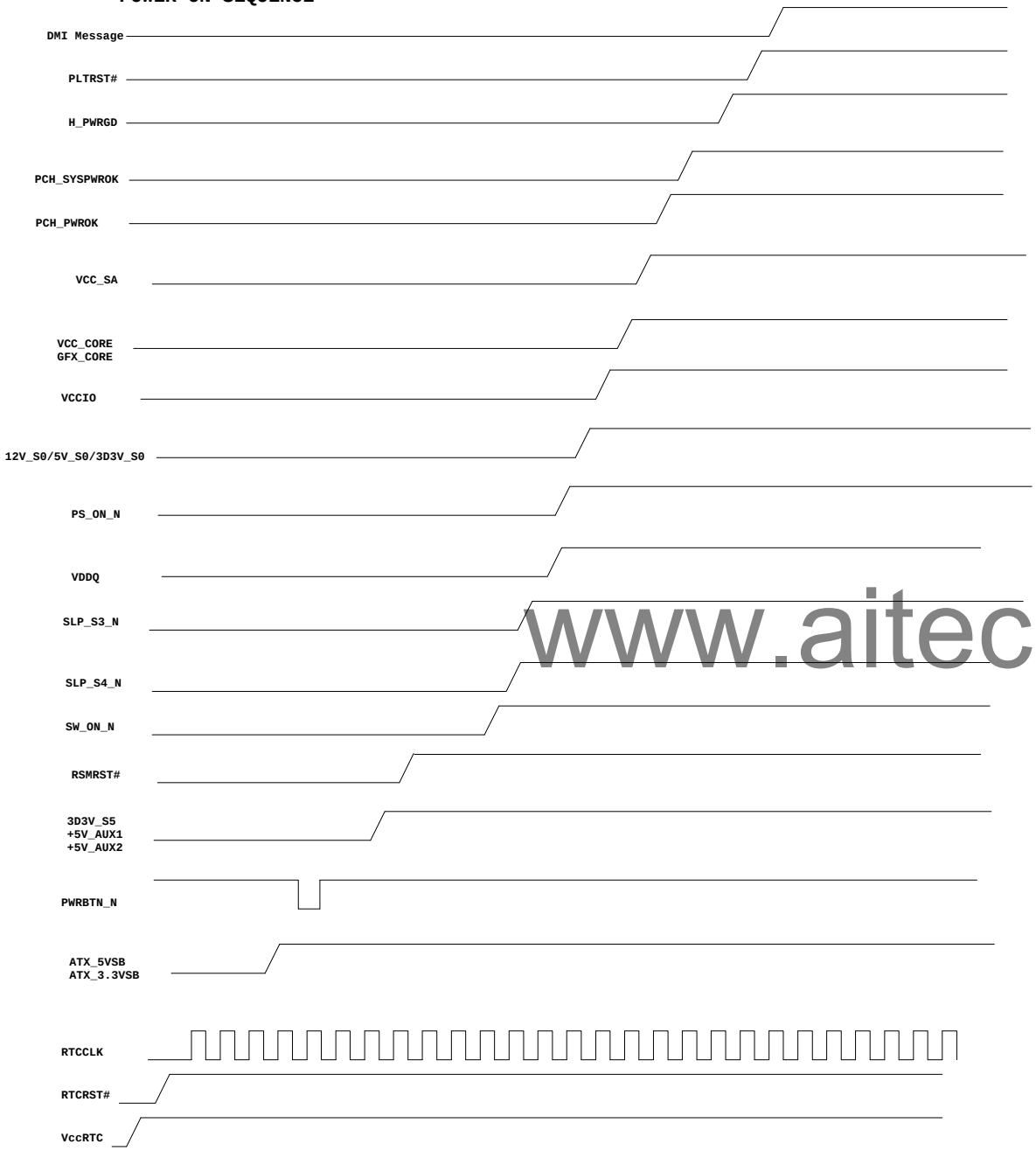
POWER ON SEQUENCE



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Title: Power sequence

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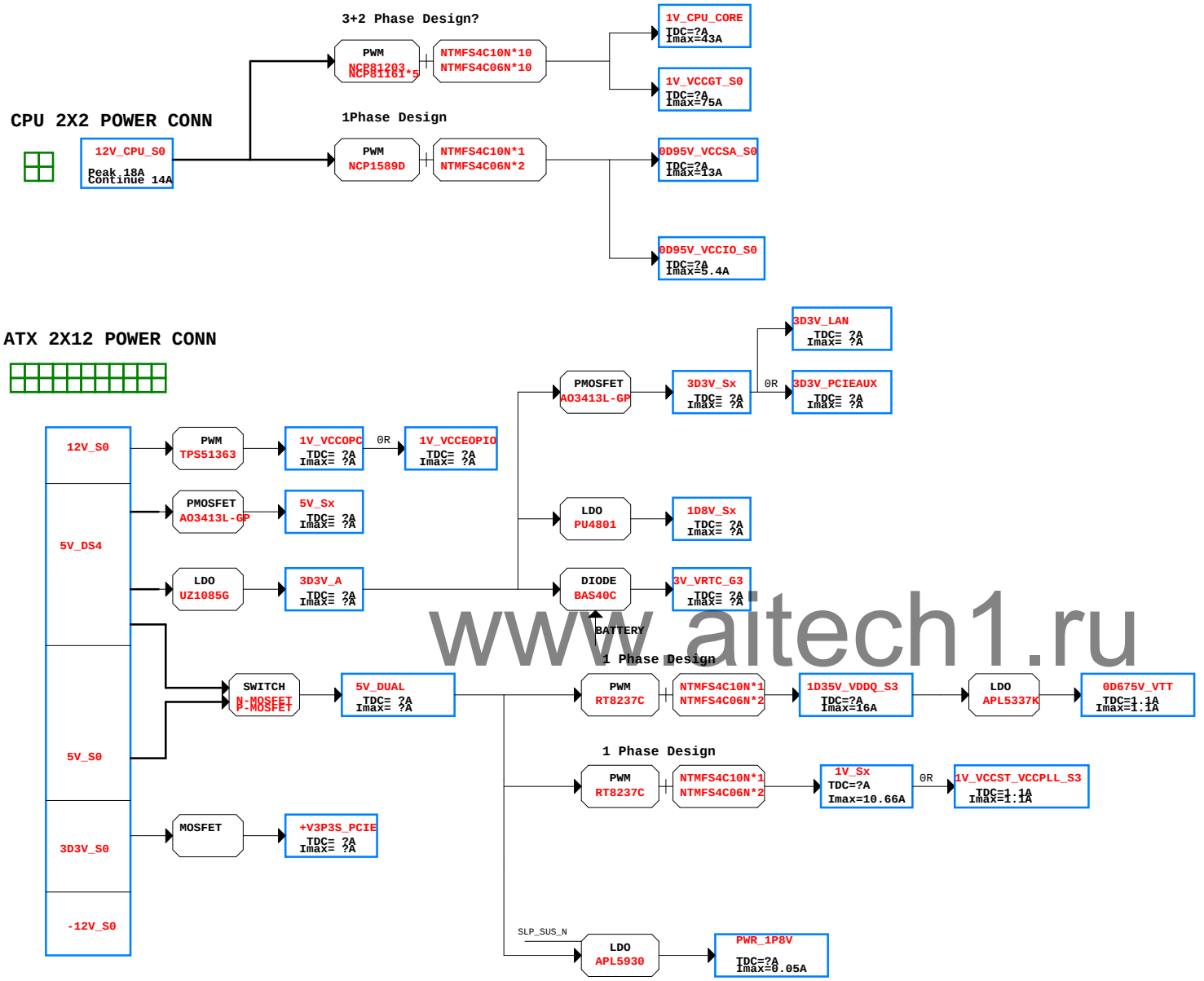

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Title: Power Block Diagram

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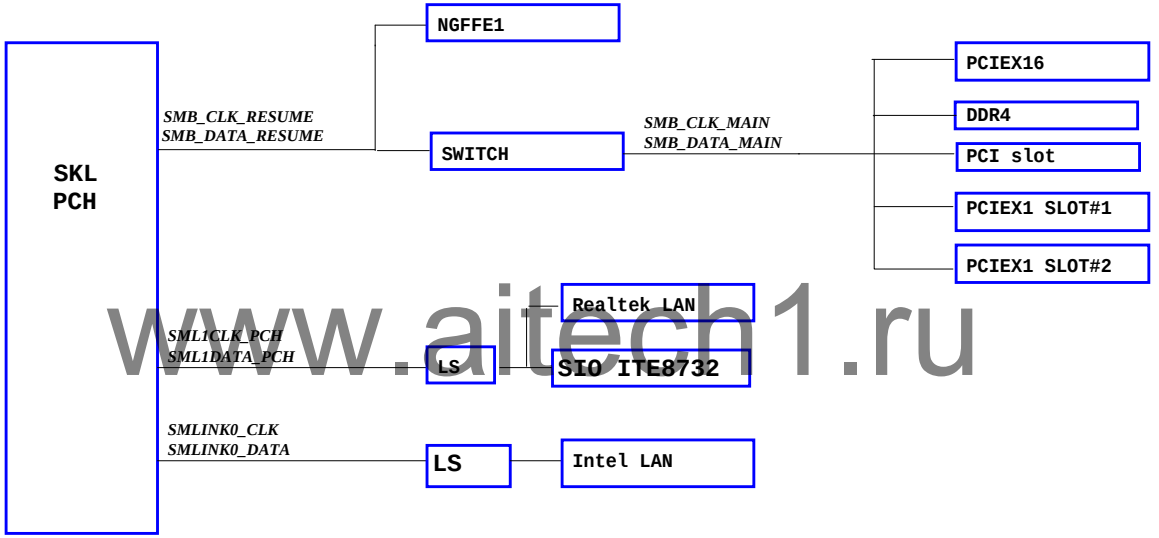

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Title: SMBUS Block Diagram

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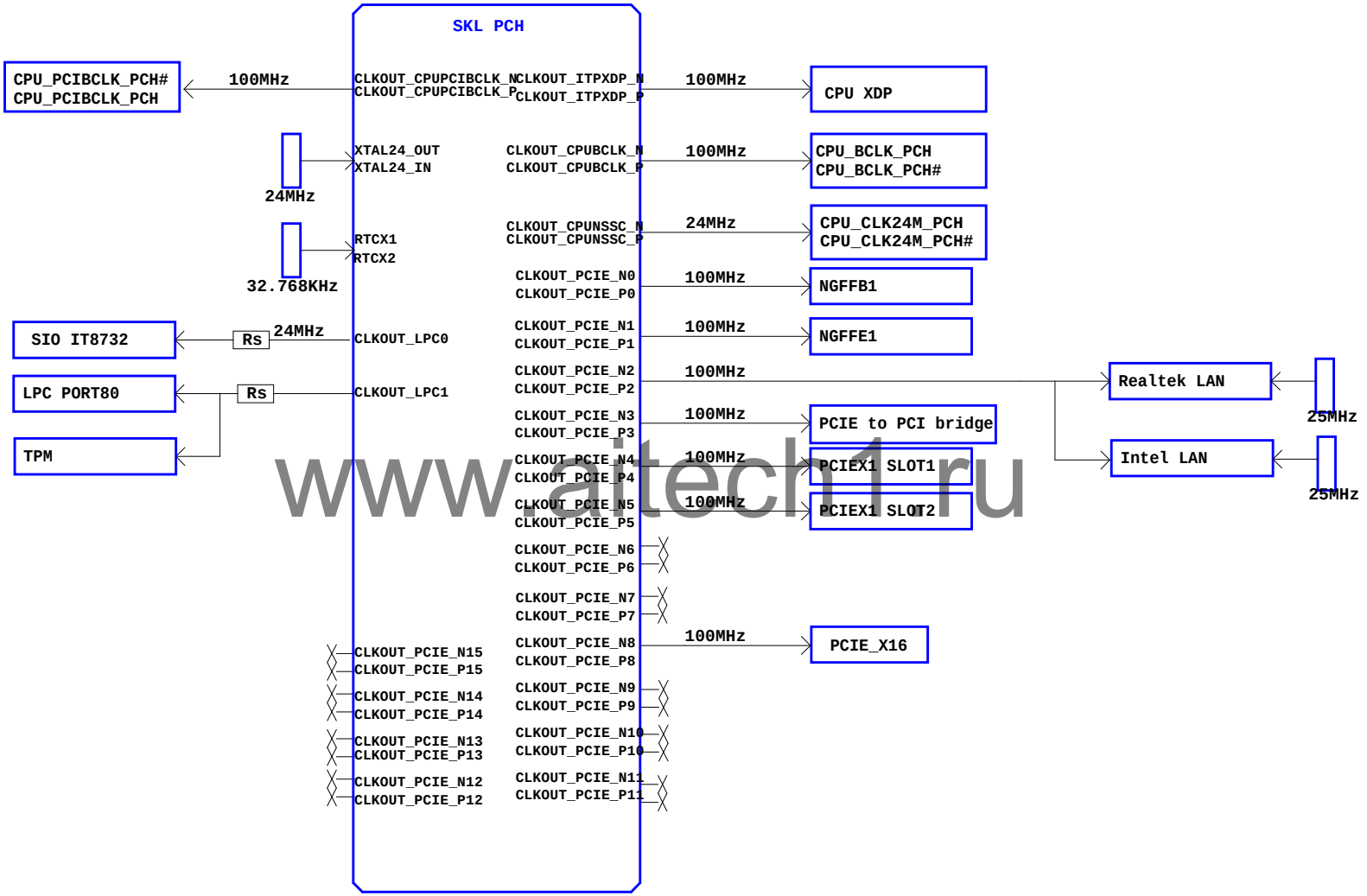

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Title: Clock MAP

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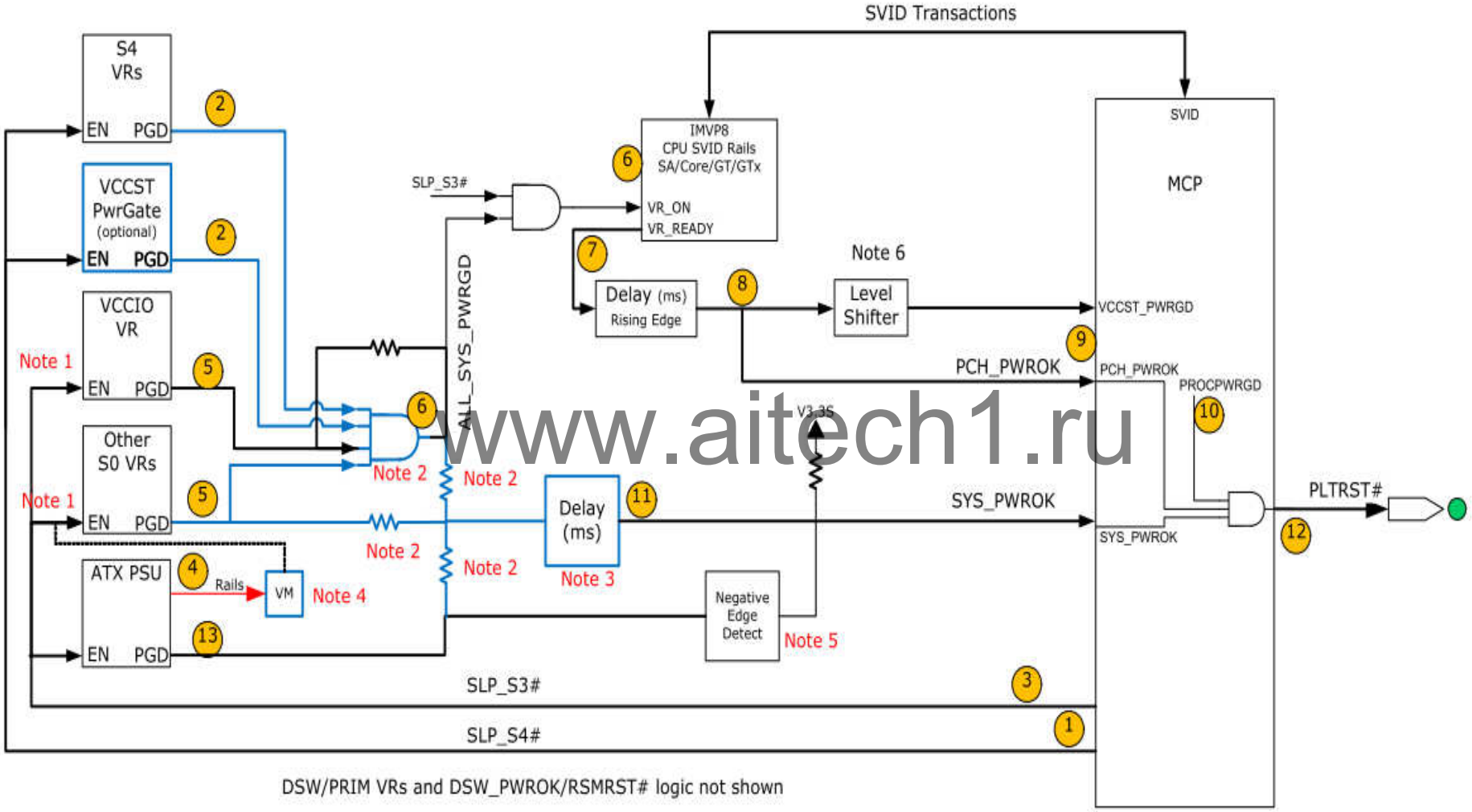

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Title: RESET Flow Chart

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Title: Change History

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